

# Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

**CONSIDERATIONS IN DESIGNING LOW-POWER, SINGLE-SUPPLY SYSTEMS** (page 3)

Maximizing battery life in communications systems (page 7)

Ask the Applications Engineer—Interfacing to serial converters (page 20)

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## Editor's Notes

### COMMUNICATING

**AnalogFax™:** As you amble through the pages of this publication, you may see an item mentioned that you'd like more details about. In the past, we've provided ways to reach us by phone and fax, and—if you can wait for the mails—via “bingo” numbers on a reply card. Now, for our North American readers, data sheets are available almost immediately via a 24-hour automated fax system that we call AnalogFax. You call 1-800-446-6212 and key in your request, using a 4-digit Faxcode; within minutes a data sheet is passing through your fax machine. Lucky North American readers! What about the rest of us? Here's an answer, in the words of Marketing Manager, Broadband Telecommunications—Rupert Baines:



### Analog Devices on The Web:

“ADI now has a home page on the World Wide Web (*EET's* ‘Best of the Web’ for 1995). It includes a plethora of information on our company, our products, and their target applications. The site is intended to help engineers throughout the design-in process. There are articles and white papers discussing the underlying technologies, search tools to help you find the ideal component for your application, and we are developing a full set of material, including data sheets on every current part—and even SPICE models and evaluation board layouts for many of them.



“One of the things you might want to try is the Signal Chains: two dozen typical applications having essentially common block diagrams, with suggestions of typical parts that are well-suited to the various roles. Others are a detailed cross-reference to other available parts and a “free text” search, so you can merely type in a keyword and find a host of (hopefully) useful pointers.


“Give it a try: <http://www.analog.com>”.

### STRADDLING THIRTY

Analog Devices, on the threshold of \$10<sup>9</sup> ( $\approx$  \$2<sup>30</sup>) in annual revenues, has just completed its 30th year in business, and this publication is about to enter its thirtieth year in print. Both have exhibited a longevity that is unusual for the electronics business. And both are highly respected and important sources—of products and information, respectively—in the markets we serve.

In this period Analog Devices op amps have progressed, from assembled encapsulated packages using arduously chosen component kits, to quads of matched high-performance IC op amps in a package smaller than the capacitors we used to use. Our product mix now ranges from classical analog—the fastest and the most-precise of op amps—to advanced digital: the fastest and most versatile of digital signal processors afloat, with on-chip memory. And we're the world's leading manufacturer of what's in between—*data converters*.

As the editor of this publication continuously for 28 of the 30 years, we've never lacked for something new and important to feature. The writing of all those issues and the interfacing with some of the great designers, technologists, and application engineers (our former *forte*) was as much a continuing education for us as the material we published must have been for our readers. And the technology we used—from

straight mechanical typewriter to Pagemaker, from U.S. Mails to The Web—paralleled the progress in our products and those of our readers. “Trees don't grow to the sky,” but each innovation seems to open up the possibility of yet more years of growth and learning. 

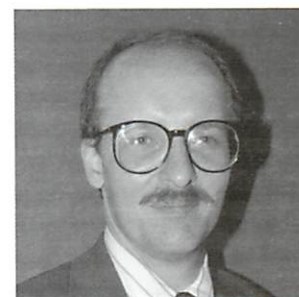
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## Analog Dialogue

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# Considerations In Designing Low-Power, Single-Supply Systems

## Part I: Designs using ac line power

By Steve Guinta

*We consider here the implications and performance tradeoffs of converting a system design using active devices (e.g., op amps, A/D and D/A converters, etc.), conventionally characterized for dual supplies, to single-supply operation. (Conventional active devices designed for optimum performance with bipolar power supplies have inherently less-than-optimum performance in single-supply operation, especially at the lower voltages.) We go on to observe the advantages in speed and dynamic performance of several new product families built on processes specifically designed and characterized for single-supply operation.*

One can't help noticing that single-supply designs are becoming very popular within the design community, because they reduce costs and take advantage of the widely available power sources commonly used in computer systems and digital/mixed-signal equipment. Many classical high-performance circuits were developed using op amps with  $\pm 15$ -volt supplies, but now single-supply operation at lower voltage is necessary in (for example) high-speed video circuits. In order to minimize power consumption in the handling of video signals, typically of the order of only 1-2 volts p-p, a 5-V single supply is used. But a conventional high speed op amp, originally designed to operate normally with  $\pm 15$ -volt supplies, would have to be operated at a considerably reduced voltage and biased at mid-supply. Reducing the supply voltage, however, reduces quiescent current, which adversely affects bandwidth and slew rate, as we will see, and may introduce "headroom" problems.

Another example in which single-supply operation is not only desirable, but essential, is in portable, battery-operated equipment. Where a battery is the primary supply voltage, minimal quiescent current is critical to extended operation. Battery-powered systems will be discussed in detail in part II of this article, which will appear in the next issue of *Analog Dialogue*.

A prime example of a battery-powered application in which low-power, single-supply devices are advantageous and essential is the "laptop" or "notebook" PC. Ten years ago, who would have thought you could carry around a system with up to 10 $\times$  the computing power and memory capability of the older benchtop PCs (at 1/10th the size and weight!)—and sporting such increased functionality as VGA Color Graphics monitors, FAX/modem and CD-ROM, yet capable of running off a battery for 2-3 hours without recharging!

Another motive for designing (or converting to) a single-supply system may be simply to reduce the cost, complexity and power consumption of an existing multi-supply design. A conventional multi-supply design, with both analog and digital circuitry, generally needs  $\pm 12$ -V or  $\pm 15$ -V supplies to power op amps, +5 V or +12 V to drive TTL or CMOS logic circuits—and perhaps both to power A/D or D/A converters. The use of an existing on-board single supply voltage (typically +5 V) to power all the components

\*For technical data on devices mentioned here, use AnalogFax™. Phone 1(800) 446-6212, and use Faxcode numbers.

can eliminate the need for costly dc-dc converters—which can consume considerable pc board space. For example, a +5 V to  $\pm 15$ -volt dc-dc converter, providing up to 200 mA of output current, might require a 2"  $\times$  2" space on the board; a similar converter with 400-mA output might require as much as 2"  $\times$  3.5" of real estate!

Increasing the reliability of the system is yet another—and not-so-obvious—advantage of single supply operation. Components operating at voltage levels much lower than their maximum rating inherently last longer. In reliability calculations, stress factor (the ratio of the device's operating voltage to its maximum rating) is included in the mean-time-to-failure (MTTF) calculations: an amplifier with a maximum rating of  $\pm 18$  volts and operating from  $\pm 15$  volts has a stress factor of 5/6, or 0.833; when operated at +5 V, the stress factor drops to 5/36 (= 0.139).

Having touched upon some of the areas where single supply operation can be beneficial or essential, let's examine in more detail some of the potential design limitations and possible tradeoffs in designing or converting to single supply operation. We will then then consider products, processes, and practices to overcome the speed and dynamic limitations inherent when conventional devices are used within a single-supply design. Although an operational amplifier is used as our model in many of the examples, the design issues and performance tradeoffs generally apply to other devices as well.

### PERFORMANCE TRADEOFFS

**Dynamic Range:** Dynamic range is perhaps the most significant tradeoff in using conventional op amps in a single-supply design. Decreased dynamic range reduces signal-to-noise ratio, which ultimately limits usable system resolution. For example, a conventional bipolar op amp operating from  $\pm 15$ -volt supplies (Figure 1 left) usually requires a fixed "headroom" of from 1.5 V to 3 V between its maximum input/output swing and the supply

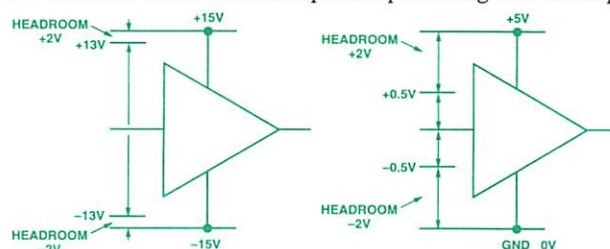


Figure 1. Illustration of headroom in relation to supply voltage.

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rails. This headroom is determined by the NPN architecture at the input stage, and by the  $V_{CESAT}$  of the output transistor stage, for a given output load condition, and changes but little with supply voltage. The op amp, operating on  $\pm 15$ -volt supplies, has an input/output range of  $\pm 13$  V.

If the supply voltage is now reduced to a single +5 V supply (Figure 1 right), the full-scale range is severely limited to  $2 \times (2.5 \text{ V} - 2 \text{ V}) = 1.0 \text{ V p-p}$ , because of the essentially fixed headroom. If one can assume that the amplifier's noise floor is unchanged, the reduction in signal swing reduces the effective dynamic range in the same proportion.

**Input Offset Voltage:** Another effect of reducing the power supply voltage is a shift in the amplifier's *input offset voltage*. The problem stems from the fact that most conventional op amps, with a typical operating range down to  $\pm 4.5$  volts, are generally tested, and have their input offset trimmed, at a specific supply voltage, e.g.,  $\pm 15$  volts. Reducing the supply voltage can produce a shift in the input offset voltage. The shift in the offset voltage can be determined by looking at the "power-supply rejection ratio" (PSRR), or "power-supply sensitivity" of offset voltage specification; it provides a measure of the change in offset for a given change in supply voltage.

For example, an OP177 has an initial offset of 20 microvolts at  $\pm 15$  volts, and a PSRR of  $1 \mu\text{V/V}$ . If the power supply is reduced to  $\pm 5$  V, the offset changes as follows:

Initial Input Offset Voltage @ $\pm 15$ V	$\pm 20 \mu\text{V}$
Power Supply Rejection Error ( $1 \mu\text{V/V} \times 20\text{-V change}$ )	$\pm 20 \mu\text{V}$
Derated Input Offset Voltage	$\pm 40 \mu\text{V}$

**Ground Reference:** Selecting a suitable ground reference also becomes critical, because, with a single supply rail and depending on the application requirements, "ground" may be anywhere within the range of the supply. For one-sided dc measurements, the negative supply rail, ( $-V_S$ ) is an excellent choice for two main reasons:

- Maximum dynamic range is achieved between the supply rails (to within the amplifier's headroom requirements)

- the negative supply rail provides a low-impedance return path for the positive supply current

For bipolar dc measurements or for ac applications, however, the choice is not as simple. A "pseudo" ground is needed to handle "bipolar" voltages or alternating excursions of the ac waveform about a "zero" value. An obvious choice for this pseudo ground (but not necessarily the best) is at a midpoint between the positive and negative (ground) supply rails. This ground can be created in various ways. A simple method for creating a pseudo ground is to use a resistive divider, as shown in Figure 2.

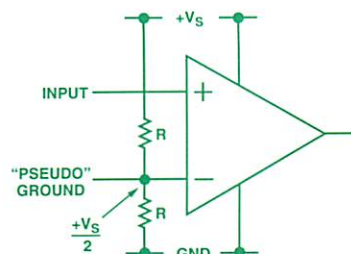


Figure 2. Simple resistive ground reference.

This approach has several problems: the inaccuracy of the ground point due to mismatch of the resistors, the drift of the resistors, and the inability to load the circuit (Figure 3). Variations of the positive supply rail will also move the ground point. And, perhaps most tellingly, it can only be used as an input ground reference, not as an output ground return.

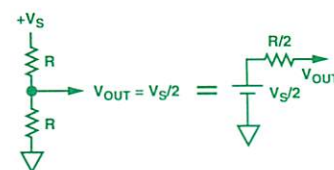


Figure 3. Equivalent circuit of resistive ground reference.

Table 1. Single Supply Amplifier Guide

Part No.-Devices/Chip	Temp			Supply Voltage				Rail-to-Rail		V <sub>OS</sub> (mV)	Slew (V/ms)	e Noise nV/√Hz	I <sub>OUT</sub> (mA)	I <sub>SY</sub> (mA)	I <sub>BIAS</sub> (nA)	GBP (MHz)	Key Feature	Faxcode\$	
	1×	2×	4×	Range	3 V	5 V	12 V	±15 V	In										Out
OP	113	213	413	I		•	•	•			125	0.9	4.7	±30	1.75	650	3.5	Low noise, low drift	1666
OP		279*		I		•	•		•	•	4000	3	22	±80	3.5	300	5	80 mA output current	1811
OP	183	283		I	•	•	•	•			1000	10	10	±25	1.5	600	5	5 MHz from +3 to +36 V	1675
OP		284	484†	H	•	•	•	•	•	•	65	2.4	3.9	±8	1.25	300	3.25	Like OP27, single supply	1871
OP	191	291	491*†	H	•	•	•		•	•	300	0.4	35	±13	0.4	50	3	Low power R-R in/out	1809
OP		292	492†	H		•	•	•			800	3	15	±8	1.2	700	4	Low cost	1697
OP	193	293	493	H	2 V	•	•	•			75	0.012	65	±8	0.015	15	0.035	Precision, long battery life	1856
OP		295	495	H	•	•	•	•		•	300	0.03	51	±18	0.15	20	0.075	Accuracy and output drive	1698
OP	196	296*	496*†	H	•	•	•		•	•	300	0.3	26	±4	0.05	10	0.35	Micropower R-R in/out	1926
AD	820	822	824†	I	•	•	•	•		•	400	3	16	±25	0.8	12 pA	1.8	FET input, low power	‡
SSM		2135		I		•	•	•			2000	0.9	5.2	±30	3.5	750	3.5	Excellent for audio	1794
											t <sub>p</sub>				I <sub>SY</sub>				
											(ns)				(mA)				
CMP			401*†	H	•	•	•			•	3000	17			7.7			23 ns comparator	1872
CMP			402†	H	•	•	•			•	3000	54			2.4			65 ns comparator	1872

Temperature Ranges I:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; H:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Packages \*TSSOP will be available; †Available in narrow SO package; ‡Faxcodes: AD820-1406, AD822-1407, AD824-1810; §Use AnalogFax™. Call 1-800-446-6212 and request Faxcodes.

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Specifications given at  $V_S = +5$  V.

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A second solution involves the use of a Zener diode or a reference regulator (Figure 4). This eliminates ground dependency on the supply rail; however, choice of Zener or regulator voltages may be limited. Its lower impedance allows it to be used as an output ground with a limited range of loads.

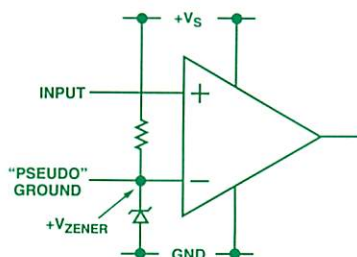


Figure 4. Zener diode as pseudo-ground.

Perhaps the most flexible approach is the equivalent of a regulator—combining a resistor divider or resistor-Zener pair, perhaps using single or stacked 1.23-V AD589s, and a low cost, general purpose op amp with appropriate output current range, used as a low-impedance ground generator.

Figure 5 illustrates the use of the pseudo-ground technique in designing a 50-Hz/60-Hz single-supply notch filter.

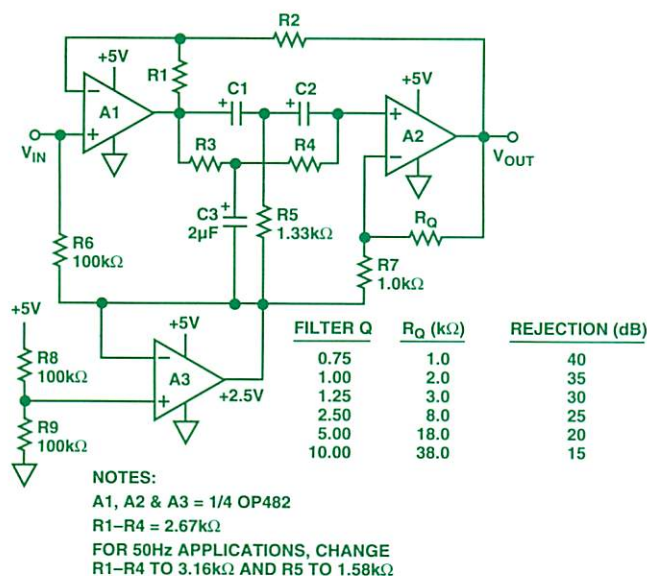


Figure 5. Single-supply 50/60-Hz notch filter.

## RAIL-TO-RAIL

A special class of amplifiers with very low headroom requirements, known as rail-to-rail amplifiers, are increasing in popularity because of their unique ability to operate with the extremes of their input and/or output ranges at or near ground and/or near the positive rail (to within a few millivolts). This significantly increases the dynamic range of the system to practically the entire range of the supply voltage.

Conventional op amp input designs (Figure 6) employ either NPN bipolar junction transistors (BJT)—which offer the advantage of high bandwidth ( $f_t$ ), lower noise and low drift, but higher current consumption—or junction field-effect transistors (JFETs), which

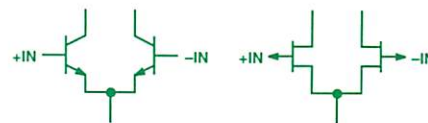


Figure 6. Conventional input stage uses paired BJT or JFET transistors.

have the advantage of very high input impedance, very low leakage (bias) current, and low distortion.

Unfortunately, both designs require operation using dual + and - supply voltages, and require 2-3 volts of headroom at either rail in order to operate effectively within their linear region.

The rail-to-rail amplifier employs a special input structure, using back-to-back NPN and PNP input transistors and double-folded cascode circuitry to allow the inputs to reach to within millivolts of either rail.

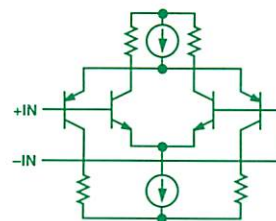


Figure 7. Rail-to-rail input stage uses back-to-back pairs of complementary transistors coupled to double folded-cascode gain stages (not shown).

The output stage of a conventional op amp (Figure 8 left) uses an NPN-PNP emitter-follower pair arranged in class AB operation. Output swing is limited by the  $V_{BE}$  of each transistor, plus the IR drop across the series resistors. The rail-to-rail amplifier output is from the collectors of an NPN-PNP pair configured as shown in Figure 8 right; the output swing is only limited by the  $V_{CESAT}$  of the transistors (which can be as little as several millivolts, depending on collector emitter currents), by  $R_{ON}$ , and by the load current.

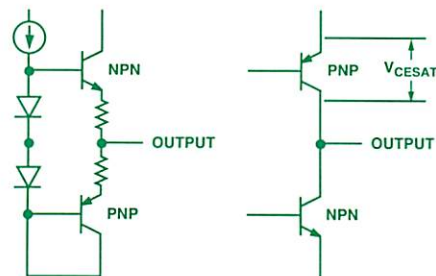
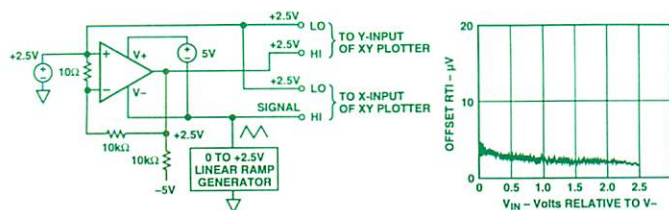


Figure 8. Conventional and rail-to-rail output stages.

An indication of how well a rail-to-rail amplifier performs is its ability to remain linear at or near zero volts. In the circuit of Figure 9a, the common-mode input to an OP90 is driven linearly through a 2.5-volt range from zero, and the amplifier is configured to multiply the resulting input error by 1000. The plot in (b) shows a small and essentially linear deviation over the 2.5-V range, without any hooks, bumps, or discontinuities, even in the vicinity of zero.





a. Test setup. b. Plot of output error, referred to input.

Figure 9. Testing linearity near the lower rail.

Table 1 (page 4) compares the specifications of amplifiers from Analog Devices for rail-to-rail applications.

**Bandwidth, Slew Rate:** Besides lowering supply voltage, the op amp manufacturer can further reduce power requirements by designing the device to require less quiescent supply current. Supply current is not strongly affected by supply voltage; it is principally under control of internal bias currents, which are established by the designer's choice of resistance in the bias circuit. In general, however, bandwidth, slew rate, and noise specifications can be adversely affected by a reduction in quiescent current. For example, a 4× increase in resistance to reduce quiescent current in a given circuit, can double the Johnson noise, which is proportional to the square-root of resistance.

For dc to low-to-mid-frequency applications, such as portable medical, geological or meteorological equipment, power consumption is the critical factor, and bandwidth reduction is of less concern. However, a video-speed amplifier, operating at reduced supply voltage in order to reduce power consumption, suffers a reduction in bandwidth and slew rate due to the reduction in its quiescent current.

What limitations does this place on the design of high-speed, low-power amplifiers? While it is true that bandwidth is proportional to quiescent or operating current, the actual ratio of bandwidth to quiescent current, MHz/mA—among other properties—is a function of the specific manufacturing process the op amp family is designed for.

Figure 10 shows the reference slopes depicting the typical relationship between bandwidth and quiescent current for Analog Devices BiFET, complementary-bipolar (CB) and eXtra-fast complementary-bipolar (XFCB) processes, with representative product types. Note that the AD8011 is capable of 300-MHz bandwidth, while drawing a quiescent current of 1.0 mA maximum from a single +5-V supply (and it generates only 2 nV/√Hz of noise at 10 kHz).

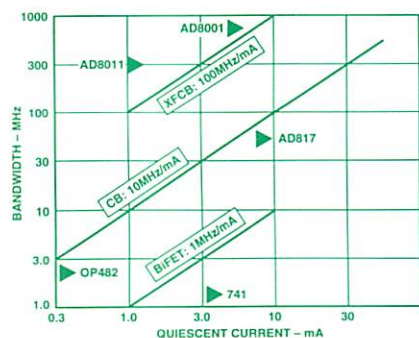


Figure 10. Bandwidth vs. quiescent supply current for IC op amps using various processing technologies.

**Power Supply Noise:** Noise on the power supply line can be a serious problem, especially in measuring low level signals. The problem is compounded by designers who, in order to reduce the need for dc-dc converters or inverters in a multi-supply system, are making use of the on-board +5-V logic supply to power op amps and data converters. The difficulty is that, in addition to having to supply output current randomly determined by changing logic and clock states, most logic supplies are derived from highly efficient, but noisy, switching supplies. Although carefully implemented logic circuitry is less susceptible to typical switching “spikes”, op amps and data converters can be seriously affected, since the spikes may appear on both the supply rail and the ground return.

It's important to note that an op amp's PSRR, specified for dc and low frequencies, degrades with frequency. Not only can spikes from the power supply appear in the amplifier's output, but—if they are sufficiently large—they may be rectified in the amplifier input stage and cause dc offsets. Similarly, for A/D and D/A converters, the switching spikes can introduce errors in their analog sections, and they may even cause clocking errors. Defenses in all cases include careful attention to board layout (number of layers, circuit locations, and restrictions on track routing), filtering, bypassing, shielding, and grounding.

Solutions can be aided by a small investment in a highly efficient LC noise filter, using Ferrite beads, as shown in Figure 11a, at the power input to sensitive circuitry. Figure 11b illustrates how the use of such a filter can virtually eliminate the “glitches” and spikes caused by pulses appearing on the power supply outputs.

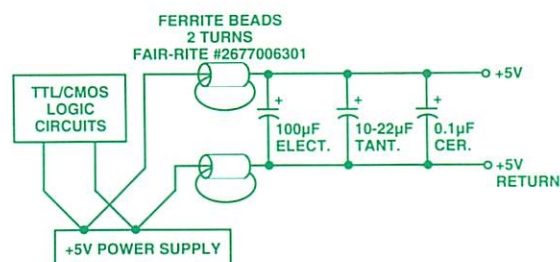


Figure 11. Filter to attenuate power-supply spikes. It should be located just outside the entrance to shielded circuit area.

We've discussed above the benefits and possible performance tradeoffs when designing a circuit or system using a single power supply, as well as products and techniques to help overcome some of the design limitations. In the next issue of *Analog Dialogue*, we'll take a closer look at some of the nuances of designing in a battery-powered system. □

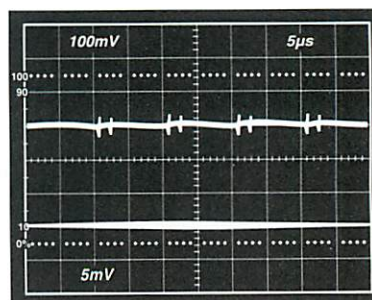


Figure 12. Spikes, “before” and “after” filtering. Note the 20× more sensitive scale.







Thus, in a typical 3-V IF design, the ADM663A/ADM666A/ADP3367 would regulate the voltage supplying the VCOs, VCO buffers, synthesizer, and driver for the PA. Allowing 750-mV (ADM663A/666A) or 60 mV (ADP3367) dropout for the regulator, plus 50 mV, the regulated voltage can be set at 2.8 V. This assumes that a synthesizer capable of operating at voltages as low as 2.7 V is available, since its charge pump should operate from a regulated voltage.

Once caveat here: there is a potential tradeoff between VCO tuning range and minimum supply voltage, since the capacitance per volt of a given varactor and the output voltage span of the charge pump might not be sufficient to provide margin for the desired tuning span. One possible solution is a charge-pump with a built in voltage doubler. For systems operating with higher battery voltages, the ADP667 low-dropout regulator accepts inputs as low as 3.5 V with 150-mV voltage drop for 200-mA output current.

In addition to using a voltage regulator to isolate devices from fluctuations in the supply, all devices operating directly from the battery must be carefully decoupled from the power supply—regulated or unregulated—in order to avoid low-frequency oscillations and current loops. For example, when creating local ac grounds at the midpoint of the supply voltage, the user may be tempted to tie several points together and use a single point as the reference (Figure 3a). A safer technique is to use isolated, individually bypassed ac grounds (b) or a low-impedance driven ground circuit (c).

Don't forget to account for voltage drops in the PC board traces and voltage drops across any R-C decoupling networks, especially for VCOs, where any change in the oscillator supply voltage or the charge pump output voltage translates into a change in frequency.

Consider also whether or not an IC has a built-in power down or must be powered down by shutting down its supply, either using an external pass transistor or powering down the regulator.

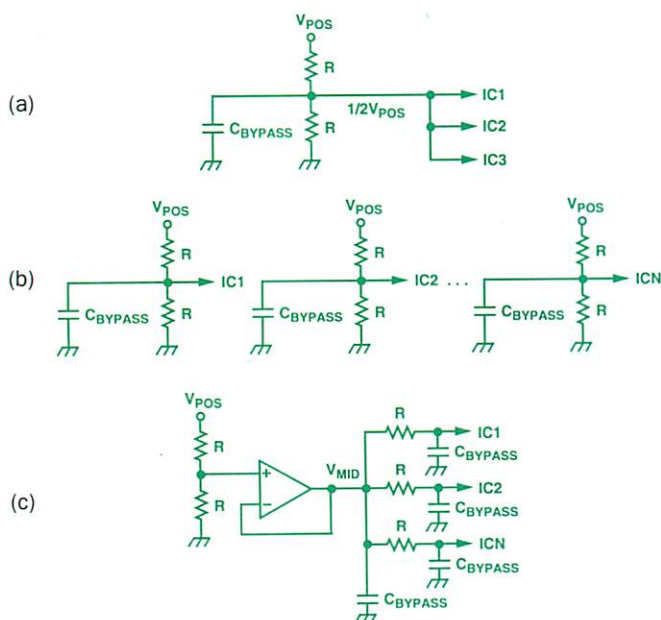


Figure 3. A single passive virtual ground is an invitation to feedback loops and instability (a). Separate, isolated grounds (b), especially when driven (c), are better. Circuit (c)'s op amp should be able to drive the capacitive load of  $C_{BYPASS}$ .

Although powering down the regulator saves power, in general, it is not wise to use its power down to turn off an individual IC to save power—the “simple” approach can cause other problems.

For example, when the supply to an IC is turned on and off, its decoupling networks must charge and discharge. The charge and discharge times add to the system's power-up and power-down times, requiring that the power be on longer than necessary just to charge and discharge the decoupling networks. Thus an IC without an internal power-down can be at a disadvantage.


But if the IC has an internal power-down, its power-supply input pin presents a high impedance to the decoupling network during shutdown, without charging and discharging the network on power-up and down or adding the decoupling network's charge and discharge time constants to the system's power up and down times.

Some ICs, like the AD607 Linear IF Subsystem IC, have internal nodes that are deliberately “held” at a specific voltage during power-down. In the AD607, the control voltage at the PLL's loop filter output is held constant during power down to minimize frequency reacquisition time upon power up.

At the system level, it is important to manage carefully which devices are powered up and especially *when* they are powered up. For example, in a cellular radio receiver, a useful order is to first power up the VCO, allow it to stabilize; then power up the synthesizer; and finally, once the synthesizer has locked, power up the rest of the Receive signal path. With this sequence, the LNA, mixer, and IF strip are left powered down until the receiver is on frequency, a process that may take several hundred microseconds. Keeping them off until the VCO is on frequency can save 400  $\mu$ s of power consumption per power up cycle.

Once the signal is demodulated down to baseband, DSP, and audio I/O, the relevant ICs can be operated from unregulated battery voltage. The mixed-signal baseband converter ICs (AD7013 and AD7015, for example) have on-board bandgap voltage-references for their bias system and multiple power-down modes to minimize power. A possible difficulty is that many of these have a minimum supply voltage specification of  $V_S - 10\%$ , i.e., 4.5 V (5-V supply) or 3-V (3.3 V supply), as do the DSPs that follow in the signal chain.

When it comes to digital signal processing, Analog Devices has a host of DSPs in the fixed-point 2100 series that operate on single +5-V supplies, including the ADSP-2171 and ADSP-2181, and the ADSP-21msp56 and ADSP-21msp59, which have on-chip analog interfaces (ADCs and DACs for voice-band signals). The ADSP-2103, ADSP-2162 and ADSP-2164 operate on 3.3-V supplies. (The ADSP-2162 and ADSP-2164 are ROM-programmed versions of the ADSP-2103.)

For audio use, the AD824 quad FET-input op amp operates at a 3-V minimum supply voltage, provides a 2-V/ $\mu$ s slew rate, operates from supplies as low as 3 V, and consumes just 500  $\mu$ A per amplifier. For better audio quality, but using more current, the AD823 dual-FET-input op amp provides a 25-V/ $\mu$ s slew rate for 5 mA per amplifier with 3-V supply. For higher-power audio output applications and 5-V supplies, the OP279 dual op amp provides a 5-V/ $\mu$ s slew rate, 80-mA output drive, and can drive a set of headphones. It consumes 2 mA per amplifier. 



# Low-Power, Low-Voltage IC Choices for ECG System Requirements

by Jon Firth and Paul Errico

## ECG Measurement from a Historical Perspective:

Electrophysical measurements have been made on humans and animals since Luigi Galvani first reported on his frog experiments in 1786. Electrocardiographic (ECG) measurements were first performed by a Dutch physician, William Einthoven, early in the 20th century. Electrocardiography refers to a commonly used noninvasive electrophysical measurement procedure for measuring, recording, and subsequently interpreting the electrical potentials that traverse the heart.

Electrodes are placed on the skin to obtain the signals of interest. Early researchers chose the hands and feet as sites for electrodes, simply immersing these extremities in buckets of salt water, from which wires were connected to a galvanometer. Subsequent research showed that metal electrodes attached to the wrists and ankles using conductive pastes obtained similar signals somewhat more conveniently.

But the equipment used at first was extremely crude, provided only basic information, with little or no storage capability and no internal diagnostic capability. Yet to come into use were the oscillograph, the vacuum-tube (and subsequently transistor- and integrated-circuit) amplifier, and the microprocessor.

**The ECG Market:** Today, ECG measurements are just a piece of the complete patient-monitoring system. Other *in vivo* bioelectric measurements include body temperature, blood pressure, blood glucose and blood oxygen levels, etc., as well as a host of off-line measurements on laboratory samples.

Today's equipment is safer and more accurate, with more internal diagnostic capability and able to operate at low voltage with battery

power—hence safe and portable.

**Low-power/Low-voltage signal-processing ICs in ECG Systems:** The first ambulatory monitoring system introduced in the U.S. over 50 years ago weighed about 50 lbs. Today's ECG systems pose but a small fraction of that weight, operate from lower voltages, and consume much less power.

Many factors drive the use of low voltage and low power for patient monitoring equipment—and consequently for low-power high-precision IC components. One of these factors is the continuing use of batteries, which have been used for decades in Holter, portable or ambulatory ECG systems. The use of low-voltage batteries as the only power source ensures that the patient (as well as the equipment) isn't exposed to "hot" line voltages under fault conditions. In addition, ambulatory ECG monitoring specifications call for 24-hour continuous recording capability; so low-power ICs are essential to maintain extended battery life.

Another driving force of increasing importance impacting on ICs for health care is the market's demand for additional functionality without increasing space, power, or cost.

**Portable Computer and Communications Markets:** Significant developments in other markets have helped provide the kinds of ICs that the medical market needs but could not support by itself. First, the explosive growth within the computer and communications markets has resulted in increased integration and decreased power consumption of semiconductors for signal processing (analog, digital, and mixed-signal). Second, similar growth within the portable consumer equipment markets has inspired a huge demand for ICs to work on single-supply voltages as low as 3.0 V, and for power-management ICs (i.e., highly efficient dc-to-dc converters and supervisory products for microprocessors). Third, long-life rechargeable batteries are now readily available. These changes have driven manufacturing volume of ICs up—and cost and power requirements down, with the benefits now enjoyed by designers for all low-power, low-voltage markets, including patient monitoring/ECG.

**ECG Equipment Architectures:** In multichannel measurement application, such as ambulatory, Holter or ECG, two basic front end architectures are in use: multiplexing analog signals into a single converter (Figure 1), and converter-per-channel (Figure 2).

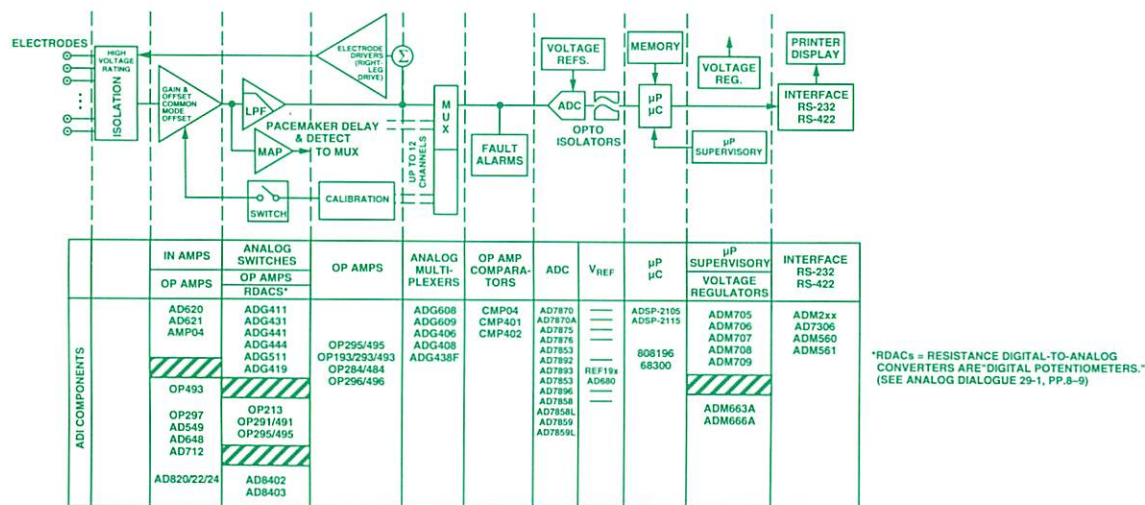


Figure 1. Typical ECG signal chain—multiplexed single-converter architecture.†

†For data sheets, use ADI's web site: <http://www.analog.com>. For immediate data on products mentioned here, find their corresponding Faxcodes on page 24, call ADI's AnalogFax™ line, 1 (800) 446-6212, and enter the appropriate Faxcodes.



The multiplexed architecture, based on an old assumption that the converter is by far the most-expensive front-end component, is prevalent in today's electrophysiological measurement systems. However, with the proliferation of sigma-delta converter architectures, converter-per-channel is now a power- and cost-competitive alternative, for rapid acquisition of high—or intelligently selected—volumes of data. Designers must now take into account all factors affecting the complete system, including power/cost trade-offs.

Let's review some important system performance requirements and their implications for the measurement electronics. The illustrations show the typical signal chains and available Analog Devices ICs that may fit requirements of the various architectures. Note that the front end amplifiers and filters of Figure 1 are repeated for each channel.

### Wide Dynamic Range

The small ac signal voltage (5 to 10 mV) detected by the sensor on the electrodes will be accompanied by a large ac common-mode component (up to 1.5 V) and a large variable dc component (300 mV). The common-mode rejection specified by the AAMI (Association for the Advancement of Medical Instrumentation) is 89 dB minimum for standard ECG and 60 dB minimum for ambulatory recorders. In low-supply-voltage systems with wide dynamic range requirements, it's important to choose low-headroom amplifiers having output voltage range approaching rail-to-rail. Examples of low-power, dual/single supply op amps and instrumentation amps ideally suited for interfacing to electrodes include:

Product	Minimum Operating Voltage Range	Quiescent Supply Current (max)	Amplifiers On Chip
<b>Operational Amplifiers</b>			
AD820/822/824*	±1.5 V, +3 V	800/800/600 $\mu$ A/amplifier	1/2/4
OP295/495*	+3 V	150 $\mu$ A/amplifier	2/4
OP291/491†	+2.7 V	350 $\mu$ A/amplifier	2/4
OP193/293/493	+1.7 V	22 $\mu$ A/amplifier	1/2/4
OP196/296/496	+3 V	60 $\mu$ A/amplifier	1/2/4
AD549 electrometer	±5 V	700 $\mu$ A	1
AD648	±4.5 V	400 $\mu$ A	2

### Instrumentation Amplifiers

AD620/AD621	±2/±2.3 V	1.6 mA	1/1
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\*Rail-to-rail output †Rail-to-rail output and input

Besides single-supply and low-power operation, key features of A/D converters for electrophysiological systems include serial interface (ideally compatible with standard microprocessors and

microcomputers), on-chip voltage reference, sleep (power-down) mode and on-chip multiplexer. Available types include:

Product	Minimum Operating Voltage Range	Power Requirement
AD7853/53L	+3 V	20/6.9 mW, sleep: <60 $\mu$ W
AD7858/58L (8-ch. multiplex)	+3 V	20/6.9 mW, sleep: <60 $\mu$ W
AD7896	+3 V	10 mW
AD7892	+5 V	60 mW
AD7893	+5 V	25 mW
AD7716 (4-A/D channels)	±5 V	50 mW max
AD7714/AD7715	+3 V	105 mW max

Figure 2 shows the converter-per-channel architecture using the AD7716 (quad, 22-bit, sigma delta ADC). The AD7716 eliminates the need for IAs and active low pass filtering. It also eliminates additional external digital control circuitry needed for multiplexed systems. In prospect are additional  $\Sigma$ - $\Delta$  devices with wider dynamic ranges, such as AD1550/51, to support converter-per-channel ECGs.

### Signal Bandwidth

The signal bandwidth will depend on whether a pacemaker pulse is being detected and whether the system is used for diagnostic (wavelength details important) vs. monitoring. In general, components of the signal of interest will reside in the 0.67 to 40-Hz bandwidth for standard ECGs and up to 300 Hz to 1 kHz for pacemaker detection.

### Right Leg Drive

Depending upon the system architecture, the electrode located on the right leg is either driven in opposition to minimize the ac common-mode voltage swings (above), or it can be used as a reference node to measure common-mode voltage for removal digitally after conversion. A suitable amplifier would be the OP97, operating on  $\geq 2.5$  V and drawing  $\leq 600$   $\mu$ A quiescent.

**Low-power digital signal processors:** Today's DSPs can now provide an attractive price/performance alternative to microcontroller/ $\mu$ P-based embedded systems. The ADSP-2173 is an example of a +3.3-V fixed-point device with on-chip memory (8 K of 24-bit program ROM, 2 K of 24-bit program RAM, and 2 K of 16-bit data RAM), suitable for low-power ECG systems.

We've described above a plethora of low-power, low-voltage ICs to fill designers' needs for most ECG applications, including patient and vital-sign monitors, diagnostic ECG, Holter (ambulatory ECG), defibrillators, and stress testers. As future systems continue to demand increased functionality and less power, new ADI ICs will exist to meet developing needs. ▶

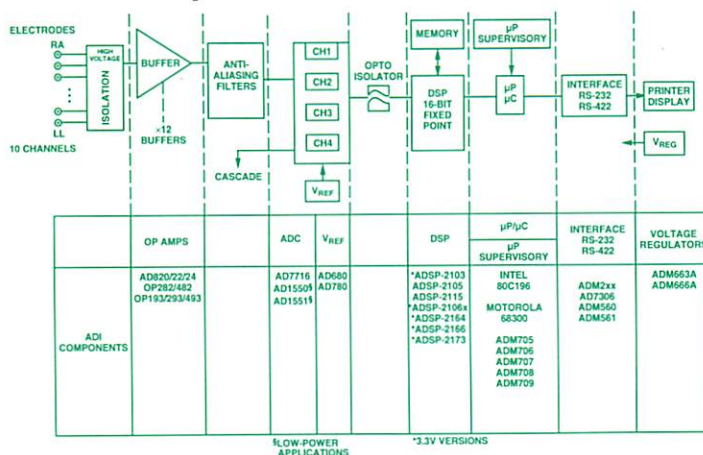


Figure 2. Typical ECG signal chain—converter-per-channel.†

†For data sheets, use ADI's web site: <http://www.analog.com>. For immediate data on products mentioned here, find their corresponding Faxcodes on page 24, call ADI's AnalogFax™ line, 1 (800) 446-6212, and enter the appropriate Faxcodes.



# Single-Supply Acceleration-to-Frequency Circuits

**A single-chip accelerometer and a V-to-F circuit ease digitizing and transmission of remote signals**

by Charles Kitchen, David Quinn, and Steve Sherman

## Introduction

A monolithic accelerometer's output can be connected to a voltage-to-frequency converter (VFC), a circuit whose output is a variable frequency, to generate a frequency proportional to acceleration simply and at low cost. The information in the resulting high-level ac signal can be sent through noisy environments having attenuation and nonlinear response—yet can be recovered reliably. For acceleration-to-digital conversion, a microprocessor can be easily programmed to read the frequency and directly compute the applied acceleration.

We will suggest here two circuits using single-supply voltage. One employs a precision high-linearity VFC, the AD654; the other uses a popular low-cost 555 timer chip.

## High-performance acceleration-to-frequency circuit:

Figure 1 shows a circuit, using a VFC, whose output frequency varies directly with applied acceleration. The circuit operates from a single +5-volt power supply.

The ADXL05 is housed in a TO-100 hermetically sealed can. Acceleration (positive or negative) sensed in the direction of the package tab is directly converted to an analog voltage. The acceleration may be associated with motion, or it may involve static measurements involving  $g$ , the acceleration of Earth gravity. For example, if the ADXL05 is mounted so that the tab's orientation is tilted with respect to the vertical, the output will depend on the in-line component of  $g$ , thus providing a measure of the tilt angle.

An on-chip buffer amplifier is available to provide scaling and offset; the accelerometer's output voltage, as the input to the AD654 VFC, controls the frequency of the output pulse train appearing at pin 1 of the AD654. Table 1 illustrates a set of scaling options for controlling the sensitivity of frequency to acceleration—and the

frequency representing zero acceleration—for various nominal values of external resistance and capacitance.

**Table 1. Nominal Circuit Component Values for Various Zero-g Frequencies and Scale Factors**

Zero-g Frequency Hz	Scale Factor Hz/g	Ct (Rt=2.49kΩ) microfarads	R3 kilohms	R2 kilohms Standard Values	R1 kilohms
10	10	10	182	464	14.70
100	10	1	49.90	127	40.20
100	100	1	182	464	14.70
1,000	10	0.10	16.50	42.20	133
1,000	100	0.10	49.90	127	40.20
1,000	1,000	0.10	182	464	14.70
10,000	10	0.01	16.90	43.20	1,370
10,000	100	0.01	16.90	43.20	137
10,000	1,000	0.01	49.90	127	40.20
100,000	10	0.001	0.169	0.43	137
100,000	100	0.001	1.69	4.32	137
100,000	1,000	0.001	16.90	43.20	137

The nominal sensitivity of the ADXL05 (voltage output at pin 8) is  $\pm 200$  mV/g, with 1.8 volts representing 0 g. The on-chip buffer amplifier (output at pin 9) increases the output offset to +2.5 V (to provide for the maximum symmetrical output voltage swing, using a +5-V supply), and also amplifies and buffers the signal. C5 and R3 provide low-pass filtering to improve low-level resolution (but limit frequency response). Gain and offset calculations are based on *nominal* values of accelerometer and VFC parameters; the actual performance is affected by device tolerances, which may be substantial. For increased accuracy of zero-g offset and scale-factor, trim potentiometer circuits can be used to predict resistance values for 1% tolerance fixed resistors.

**Nominal design equations:** The output of the AD654 is a pulse train whose frequency is related to the input voltage by:

$$f_{out} = 0.1 V_{IN} \left( \frac{1}{R_t C_t} \right)$$

Thus, for a 0-g output of 2.5 V from the ADXL05, the frequency corresponding to a zero acceleration is

$$f_{0g} = \frac{0.25}{R_t C_t}$$

The scale factor, or slope of the relationship, expressed in Hz/g, is the product of the sensitivity of the accelerometer (200 mV/g), the gain of the buffer amplifier, and the VFC relationship, or

$$SF = \Delta f / g = 0.2 \frac{R_3}{R_1} \left[ \frac{0.1}{R_t C_t} \right]$$

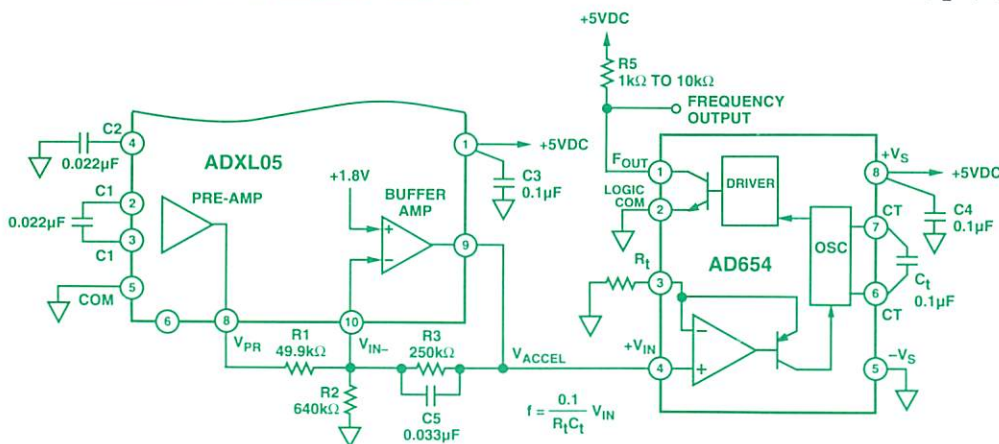


Figure 1. High-performance acceleration-to-frequency circuit using the high-linearity AD654 VFC.




The accelerometer may be self-calibrated, using the Earth's gravity. With the accelerometer's tab horizontal, the accelerometer will measure 0 g, allowing the 0-g offset to be adjusted. With the accelerometer's tab pointing straight down, the output voltage at pin 9 will correspond to +1 g. If the accelerometer is rotated so that the tab points straight up, its output will measure -1 g. The difference in the readings, 2 g, can then be used to set the acceleration-to-frequency overall scale factor, using an adjustable Rt, i.e., replacing it by a fixed 1% resistor in series with an empirically established trim value.

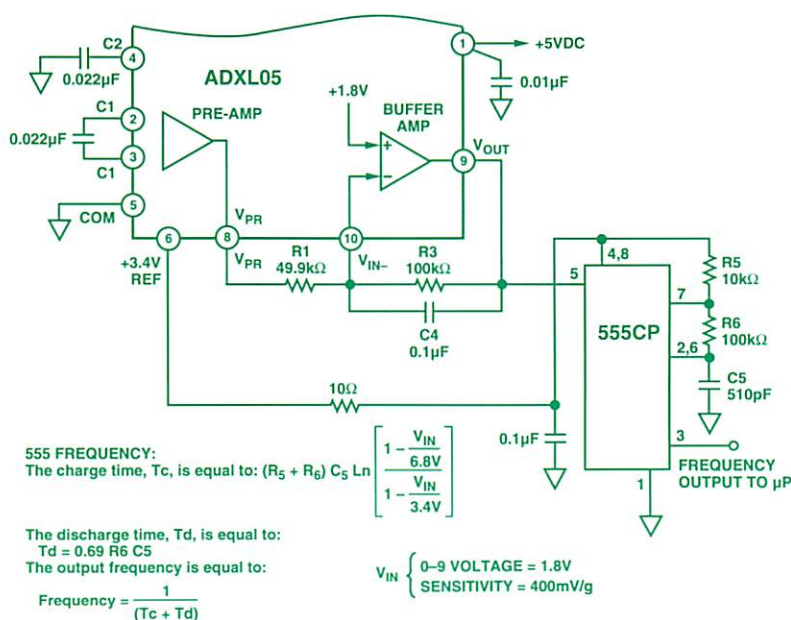
replaced by fixed resistors for dynamic measurements that might affect pot settings.

Figure 3 shows how an ADXL05 accelerometer can be connected to a low-cost CMOS 555 timer to provide a frequency output. The component values indicated were selected for a  $\pm 1\text{-g}$  tiltmeter application.

The CMOS 555 operates as a voltage controlled oscillator, where R5, R6, and C5 set the nominal operating frequency. Resistors R5 & R6 were chosen to give an approximate 50% duty cycle with a +1.8-V (0-g) input signal applied to pin 5 of the 555. To minimize any change in frequency due to supply variations, the 555 operates ratiometrically from the accelerometer's +3.4-V reference rather than directly off the +5-V supply.

Using the circuit and component values shown in Figure 3, the nominal output scale factor at pin 9 of the accelerometer will be  $\pm 400 \text{ mV/g}$ , so the voltage output will be  $+1.8 \text{ V} \pm 0.4 \text{ V}$ . The output scale factor at pin 3 of the 555 will be approximately  $16,500 \text{ Hz} \pm 2,600 \text{ Hz per } g$ .

Frequency stability of this circuit was found to be quite good. Using the circuit of Figure 3 with a 15.5-kHz 0-g frequency, the measured 0-g frequency drift over the 0 to +70°C commercial temperature range was 5 Hz/°C, which is 0.03%/°C. The change in frequency vs. supply voltage is less than 10 Hz with a +5.0 to +9.0-volt supply range. 



12



# Very Low Voltage, Micropower Amplifiers ( $V_S < 3\text{ V}$ , $I_{SY} < 500\text{ }\mu\text{A}$ )

## Choosing and using them

by Steve Sockolov

Portable medical monitoring instruments, hearing aids, and safety monitoring equipment are all examples of products that must operate from batteries and continue operating for very long periods of time. Because of size limitations, available power is severely constrained in terms of both supply voltage and current.

Amplifiers for these applications must operate from these low voltages and draw very little current. In addition, their input and output signal ranges should be as wide as possible to obtain sufficient dynamic range (full-scale signal-to-noise). The best devices will have an output voltage that can swing from the positive supply to ground and input ranges that can even exceed the power-supply range. Amplifiers capable of reaching both supply "rails" are called rail-to-rail amplifiers.

To select amplifiers for these applications consider first the required performance rather than the manufacturing process. Low-power products are available in CMOS, bipolar and JFET processes, but you should not go by preconceptions about the range of performance each is capable of.

Until recently, CMOS low voltage designs were not practical for precision low-voltage operation. CMOS processes had relatively high threshold voltages, in the range of 1.8 to 2.1 volts. Since most amplifier designs required at least two  $V_{THS}$  to operate, the minimum supply voltage was  $> 3\text{ V}$ , even at room temperature.

Bipolar designs, like CMOS, require at least two transistor drops; but these drops are  $V_{BE}$ s, so operation on 1.8 volts is quite practical. Amplifiers such as the OP293\* dual op amp are guaranteed to operate at 2 volts, and they work well down to 1.7 volts. However, care must be taken to assure that functionality will be maintained at cold temperatures, because  $V_{BE}$  increases (at about  $-2\text{ mV}/^\circ\text{C}$ ) as temperature decreases. Thus, operation at  $-25^\circ\text{C}$  will require an extra 100 mV, or more, of headroom beyond the minimum room-temperature operating voltage.

Currently, there are no JFET op amps with both rail-to-rail inputs and outputs; the AD820 family comes closest with its rail-to-rail outputs. JFET op amps can be very advantageous in applications calling for low noise, low bias current or wide bandwidth.

**Limitations of micropower designs:** Compared to standard op amps, low current amplifiers are relatively limited with regard to bandwidth, output drive, and noise level. Values for each parameter depend on the technology available during the design. Today, micro-power amplifiers can achieve speed/power ratios of  $10\text{ kHz}/\mu\text{A}$ ; and this will more than double within the next year. Therefore it is possible to build amplifiers with more than a megahertz of gain-bandwidth product, operating on less than  $100\text{ }\mu\text{A}$  of supply current. The OP496 (see page 16) is an example of what is possible today; it has a GBP greater than  $300\text{ kHz}$  while using only  $45\text{ }\mu\text{A}$  of supply current.

Amplifier broadband noise depends on front-end current, transistor size, and processing. Because of their low power and

generally smaller geometry, low-power designs generally are relatively high in input-referred noise. Again, the OP496 family, with its  $26\text{ nV}/\sqrt{\text{Hz}}$ , demonstrates the capability of today's technology.

Output drive is largely dependent upon the current available to drive the amplifier's output stage. Unlike standard amplifiers, rail-to-rail designs cannot use Darlington or similar configurations to boost current. The increased voltage drops associated with high current flow are unacceptable in these designs, so output drive is often limited to microamperes; but some product designs (such as the OP293\*) can output  $\pm 8\text{ mA}$ , even though it requires only  $25\text{ }\mu\text{A}$  of quiescent supply current.

An additional output requirement is the ability to *sink*, as well as source, current. This will enable the output to slew at the same speed in both directions. If the output cannot sink current, pull-down resistors would need to be added. This would, of course, use unnecessary current and defeat the purpose of using such amplifiers to conserve power.

### Determining the limits of proper operation at low voltages:

Here are three convenient ways to determine if an amplifier is truly working when the voltage is reduced: the *sine-wave test*, the *offset-voltage test*, and the *supply-current test*. The first two tests are useful for checking ac and dc performance, respectively; the third is a general-purpose test.

The sine wave test is the easiest of these tests. Connect the amplifier for a gain between one and two and supply an input sine wave that is within the common mode range of the amplifier. Either look at the output waveform on an oscilloscope or measure it for distortion. As the supply voltage is decreased, there is a point at which the waveform will become obviously distorted. Just before this point is reached is the minimum operating voltage.

To perform the offset-vs.-supply-voltage test, connect the amplifier in a high gain configuration and ground the inputs. Gain should be set so that the amplified offset at the output is about one volt. Start with a supply voltage for which the amplifier is known to operate properly, then measure and record the output (offset). Decrease the supply and continue to record supply voltage and offset. When these values are plotted, and as the supply is decreased further, you will usually see a knee in the plot where the offset deteriorates rapidly, just below the minimum supply voltage for proper operation.

As operating voltage is reduced, internal biasing circuits begin to shut down. At first glance, the amplifier will still appear to work, but performance can degenerate substantially. Furthermore, additional structures may shut down as voltage is further decreased. Since the amplifier's supply current is affected by these changes, it can act as a proxy for progressive changes that may be harder to observe in a particular aspect of performance. To determine these points, plot supply current against supply voltage. There are likely to be several bends in the curve, each indicating further degradations.

## APPLICATIONS

**Micropower telephone headset:** Headsets can be operated from battery power using the OP296\* with two 2.5 volt supplies. Select a headphone that has  $600\text{-}\Omega$  impedance to keep the current drain low. This circuit will work well down to 2 volts. As the figure shows, distortion is below 1% to 5 kHz.

\*The OP493 and OP496 quads (p. 16) are representative of the OP193/293/493 and OP196/296/496 families of singles/duals/quads.



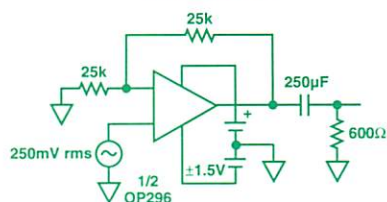
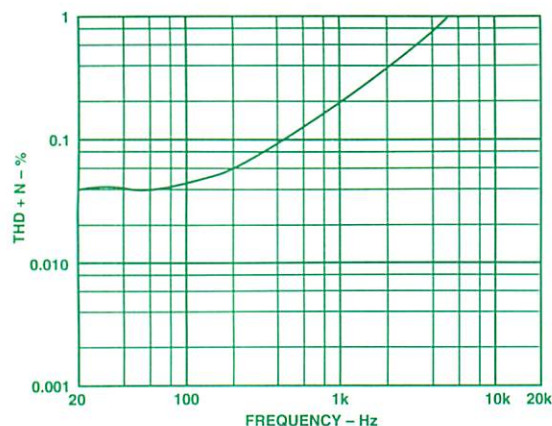


Figure 1. Headphone amplifier, with plot of total harmonic distortion.

**Pulse monitor:** ECG monitors require isolation to protect patients from any possible failure that could allow dangerous currents to flow through the body. Using a very low power amplifier, an electrocardiograph amplifier—used as a pulse monitor—could be powered from a source so weak that it could not supply dangerous current levels. As an example, here is a circuit that could be used for sports or other monitoring (but is not intended to be used in life-support systems).

There are three inputs to this circuit—from a set of measuring electrodes—a pair of sense inputs and a reference return input.

The front end is a standard three-amplifier differential circuit. Gain for the first stage is set by  $R_G$ . Gains of 50 to 150 work well. Resistance values are chosen somewhat higher than usual to reduce current consumption. The output stage has a gain of 10 V/V and should be set to roll off at 400 to 1000 Hz, fast enough to pass an ECG wavelshape, but with high-frequency noise filtered out.

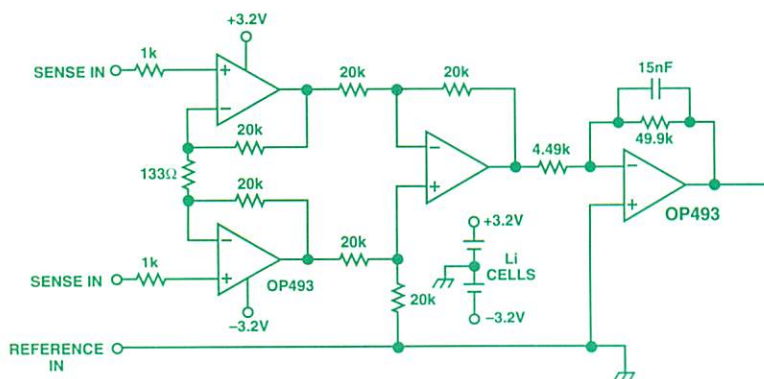
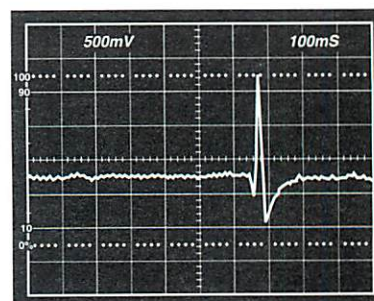


Figure 2. Pulse amplifier, with typical waveform.



The circuit requires careful layout because of the high gain and low signal levels. All leads should be kept short to reduce induced noise. The two sense inputs should be a twisted pair, shielded by the reference lead.

This pulse monitor circuit is designed to operate from two small lithium batteries, so that it may be used in portable applications, such as sports monitoring, for an extended period of time. The OP493\* is guaranteed to operate with supplies as low as 2 V, and total supply current is only 100  $\mu$ A, insuring long battery life. (For example, lithium cells are rated at 3.6 to 4.2 volts, but they are still supplying current when discharged to one-half their nominal voltage.)

**Comparator:** Amplifiers are often used as comparators, because of the convenience and availability of amplifiers with a wide variety of specifications. It's often easier to find an amplifier to meet a given set of criteria in a precision comparator application, especially where low power is essential. The newer amplifiers, with rail-to-rail inputs and outputs make excellent comparators, requiring no more components than a simple gain block.

With the OP196\* in the non-inverting configuration shown, a precision comparator, with a rail-to-rail input range can be designed, using a supply current of only 50  $\mu$ A. Typical falling- and rising-edge propagation delays are 12  $\mu$ s and 20  $\mu$ s, and a clock rate of 25 kHz is attainable. With  $R_1 = 10$  k $\Omega$  and  $R_2 = 1$  M $\Omega$ , the hysteresis measures about 70 mV. With  $R_1$  near 0  $\Omega$ , the hysteresis is only about 100  $\mu$ V.

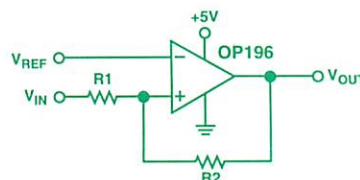


Figure 3. Non-inverting comparator.



# 10-Bit Quad DACs for Single-Supply 3.0 V to 5.5 V Operation

## Serial AD7804 & parallel AD7805 are double-buffered, have rail-to-rail output capability, plus Standby and Power-Down modes

The monolithic AD7804 and AD7805\* comprise four 10-bit voltage-output digital-to-analog converters. The **AD7804** (Figure 1) has a 3-wire serial digital interface, and is housed in a 16-pin DIP or SO. The **AD7805** can load 10 bits in parallel—or in two bytes (8 + 2) on an 8-bit bus; it is packaged in a 28-pin DIP, SO, or SSOP. The devices operate from a 3.3-V ( $\pm 10\%$ ) to 5 V ( $\pm 10\%$ ) supply, i.e., from 3 V to 5.5 V, with an output circuit that can swing from rail to rail.

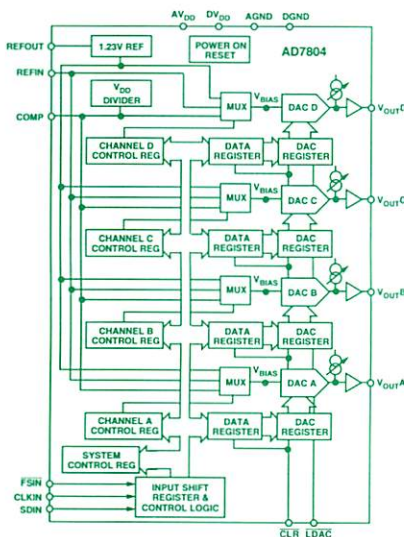


Figure 1. AD7804 functional block diagram.

The all-CMOS AD7804 and AD7805 conserve power. Besides having low dissipation (66 mW max) in normal operation, they are rated for 1.38 mW max in System Standby (with only the reference operating)—and 8.25  $\mu$ W max (over temperature) in Power-Down. In addition, the four channels can be switched individually into Standby when not in use. Each channel has a Channel-Control register to control its functions; and a System Control register controls all four DACs simultaneously.

These devices have flexible voltage referencing. A 1.23-volt internally generated reference is available at REFOUT. Under control of the channel register, the reference input for each DAC (called  $V_{BIAS}$ ) is multiplexed between the internal reference source, a REFIN terminal (for an external reference), and one-half the supply voltage ( $V_{DD}/2$ ). The voltage chosen,  $V_{BIAS}$ , provides the offset "zero" required for bipolar signals in single-supply circuitry; and the DACs are scaled for an output span of  $1.875 V_{BIAS}$ . The table shows significant points along the transfer function for twos-complement coding.

\*For data sheets, use ADI's web site: <http://www.analog.com>. For technical data, use card (Request 1) or AnalogFax™ [1-800-446-6212]. (request Faxcode 1830)

Digital Input MSB . . . LSB	Analog Output
01111 11111	$V_{BIAS} (1 + 1.875[511/1024])$
01111 11110	$V_{BIAS} (1 + 1.875[510/1024])$
00000 00001	$V_{BIAS} (1 + 1.875[1/1024])$
00000 00000	$V_{BIAS} (1)$
11111 11111	$V_{BIAS} (1 - 1.875[1/1024])$
10000 00001	$V_{BIAS} (1 - 1.875[511/1024])$
10000 00000	$V_{BIAS} (1 - 1.875[512/1024])$

The AD7804 and AD7805 have an additional facility for independently adjusting the offset of each output (i.e., locating the output value corresponding to  $V_{BIAS}$  at an arbitrarily set level). It is an 8-bit sub-DAC (shown in Figure 1 as a variable additive source in each output circuit)—with a sensitivity of 1/16 that of the main DAC. That is, each LSB change of the sub-DAC adds or subtracts  $V_{BIAS}/4096$ , with a range of about  $\pm 3\% V_{BIAS}$ . Settings for the sub-DACs are data inputs under the control of each Channel-Control register.

The DACs are double-buffered; this makes it possible to load the registers, one at a time, then simultaneously update all DAC outputs asynchronously. The DAC outputs may be cleared all at once by the System Register or individually by the Channel Control registers. The 3-wire serial interface allows direct interfacing to SPI, QSPI, and Microwire standards.

Brief specifications for B grades include  $\pm 3$  LSB max relative accuracy error,  $\pm 35$ -mV offset and full-scale gain error, 4  $\mu$ s max settling time to 1%, 0.002%/° power-supply rejection, 2.5 V/ $\mu$ s slew rate, and 1 nV-s glitch impulse. The specified operating temperature range is  $-40$  to  $+85^\circ\text{C}$ . Prices (1000s) for the AD7804 and AD7805 are \$5.75 and \$6.25, respectively.

## APPLICATIONS

The low power requirements, as well as the low cost and small size of the AD7804 (and to a slightly lesser degree, the AD7805) make them suitable wherever multiple 10-bit (or upgraded 8-bit) DACs are needed. Typical areas include voltage setpoint control, trim potentiometer replacement, automatic calibration, and other instrumentation and test functions. The serial AD7804 can be easily isolated in situations where noise, safety requirements, or distances must be dealt with. Figure 2 shows an opto-isolated interface, where the clock, frame sync, and serial data inputs are isolated by optocouplers. Each DAC is automatically updated following the 16th serial clock of a write pulse.

These DACs were designed by Hans Tucholski, in Limerick, Ireland. ▀

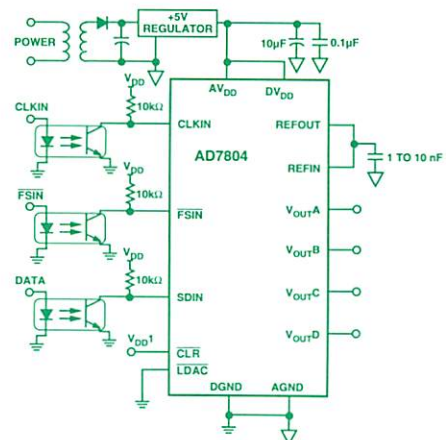


Figure 2. Serial DAC in an opto-isolated interface configuration.




## Single-Supply Op Amps: Precision Quads and Fast Single Op Amp with Disable

### 160-MHz V-feedback AD8041 for +3, +5, and $\pm 5$ -V supplies

### Trio of Quad Precision Low-Power OAs OP493: 20 $\mu\text{A}$ per amplifier channel; OP484: low noise (3.9 $\text{nV}/\sqrt{\text{Hz}}$ ); OP496 has wide swing, draws low current

The AD8041 is a low-cost 160-MHz voltage-feedback op amp that can operate from a single supply of +3 to +12 V or dual supplies of  $\pm 1.5$  V to  $\pm 6$  V. It offers true single-supply capability; its input range extends 200 mV below ground in single-supply mode; and the output voltage typically swings to within 100 millivolts of both rails with 1-k $\Omega$  load (see maximum specs and other data in table).

Dynamically, its -3-dB frequency is 160 MHz as a unity-gain follower, and it has excellent differential gain and phase for video applications: 0.03% and 0.03°. Settling time is 35 ns to 0.1% (55 ns to 0.01%). Total harmonic distortion is typically -72 dB (5 MHz,  $R_L = 1$  k $\Omega$ ). A Disable feature (120/230-ns off/on time) allows quiescent current to be reduced by 60% or more. With available output current of 50 mA, typical applications include high-speed data modems, wireless communication, and video. A dual (AD8042) and quad (AD8044) are also available. 


The OP493, OP484, and OP496 each comprise four independent precision operational amplifiers capable of operating on a range of single- or dual supply voltages, including +3 and +5 volt single supplies. Some of their key specs are compared in the table below. They are specified over the HOT industrial temperature range, -40 to +125°C, and are available in plastic DIPs and SOICs at prices as low as 52.5¢ per channel.

The OP493 is a very low power precision quad op amp, typically drawing 14.5  $\mu\text{A}$  in 5-volt operation and a maximum of 22  $\mu\text{A}$  (over temperature) with a 3-volt supply. It will operate at voltage as low as 1.8 V, with guaranteed specifications at 2.0 V. It is used wherever high accuracy at extremely low power is required. Prime uses are in applications that demand long battery life.

It features low offset and drift (total offset of 375  $\mu\text{V}$  over temperature), and low bias current (20 nA max).

The OP484 comprises four fast, accurate, low-noise amplifiers with rail-to-rail inputs and output. It can function on a single supply voltage as low as +1.5 V, with guaranteed operation from +3 V (or  $\pm 1.5$  V) to +36 V (or  $\pm 18$  V).

With  $V_{OS}$  in the range of 200  $\mu\text{V}$  over temperature, 3.9  $\text{nV}/\sqrt{\text{Hz}}$  noise, rail-to-rail input and output, and 3-MHz gain-bandwidth (unity-gain stable), the OP484 stands virtually alone in its suitability for both dc and dynamic performance in low-voltage instrumentation and control.

The OP496, the lowest-cost device in this group, features micropower operation (60  $\mu\text{A}$  max), rail-to-rail input and output, low bias current, and 450-kHz gain-bandwidth. Typical applications include monitoring low-power sources and control of battery charging. Automotive and battery-powered applications benefit from its accuracy and speed-power ratio. 

Amplifier Comparison

	OP484E/F			OP496			OP493E/F				AD8041		
Supply voltage, V	+3	+5	$\pm 15$	+3	+5	+12	+2	+3	+5	$\pm 15$	+3	+5	$\pm 5$
Current per channel, mA max	1.15	1.25	1.75	0.05	0.06	0.06	0.02	0.022	0.014 typ	0.03	5.6	5.8	6.5
Specified temperature range													
$T_{MAX}$ , °C	+125	+125	+125	+125	+125	+125	+125	+125	+125	+125	+85	+85	+85
$T_{MIN}$ , °C	-40	-40	-40	0	-40	-40	-40	-40	-40	-40	-40	-40	-40
$V_{OS}$ over $T_{MAX}-T_{MIN}$ , $\mu\text{V}$ max	200/450	175/450	300/500	650	650	650	225/375	225/375	225/375	225/375	8000	8000	8000
$I_B$ over $T_{MAX}-T_{MIN}$ , nA max	500	500	500	$\pm 30$	$\pm 30$	$\pm 30$	15/20	15/20	15/20	15/20	3000	3000	3000
Noise, $e_n$ , $\text{nV}/\sqrt{\text{Hz}}$ @ 1 kHz	3.9	3.9	3.9	2.6	2.6	2.6	6.5	6.5	6.5	6.5	16 <sub>(10 kHz)</sub>	16 <sub>(10 kHz)</sub>	16 <sub>(10 kHz)</sub>
Output saturation voltage, mA:													
$V_{S+}-V_{OH}$ , mV, max	150	150	200	150	150	150	NS	1	1	1	1 k $\Omega$	1 k $\Omega$	1 k $\Omega$
$V_{OL}-V_{S-}$ , mV, max	125	125	125	70	50	70	NS	900	900	900	300	250	400
							NS	400	400	400	450	350	550
Gain-bandwidth, MHz, typ	3	3.25	4.25	0.35	0.35	0.45	0.025	0.025	0.035	0.035	150	160	170
Slew rate with $R_{LOAD}$ , $\Omega$ :													
Volts/microsecond, typ	NS	2k	2k	100k	100k	100k	2k	2k	2k	2k	2k	2k	2k
	NS	2.4	4	0.25	0.3	0.3	0.01	0.01	0.012	0.015	150	160	170
Number of channels	4			4			4				1		
Packages	14-lead plastic DIP, SO			14-lead plastic DIP, SO			14-lead plastic DIP, 16-lead SO				8-lead plastic DIP, SO		
Prices (1000s) start at:	\$7.63/\$5.27			\$2.10			\$2.73				\$1.50		
Faxcode*	1871			1926			1856				1925, 1929 (dual), 1940 (quad)		

\*For data sheets, use ADI's web site: <http://www.analog.com> or AnalogFax™ automated delivery system: (800) 446-6212.

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## Three Fast Single-Supply A/D Converters

### 10-Bit 40-MSPS ADC

**AD9050: +5-V, 400 mW max 55-dB SNR at 10.3-MHz  $A_{IN}$**

The AD9050 is a low-cost, complete 10-bit monolithic sampling A/D converter with on-board track-and-hold and reference. It is designed for high performance at low cost and requires only an encode signal to achieve sample rates up to 40 MSPS with 10-bit resolution. The encode input is TTL/CMOS compatible, and the parallel digital outputs are CMOS. The digital inputs and outputs can be configured for 5-V or 3-V logic.

Optimized for wide-bandwidth, high-dynamic-range applications, it is useful in a wide range of applications, including medical ultrasound imaging, professional video, and digital communications. It uses a single +5-V supply, drawing 315 mW (400 max) at 40 MSPS and 10.3 MHz input, providing 55-dB typical (53-dB min) SNR and -67-dB typical (-60 dBc max) harmonic distortion. It has an analog bandwidth of 100 MHz, useful in undersampling applications.

The AD9050 is available in 28-pin SO (BR) and SSOP (BRS) packages, with an operating temperature range of -40 to +85°C. To simplify design-in problems, an evaluation board—AD9050/PCB—is available at reasonable cost. ▶

### 12-Bit, 3-MSPS A/D

**AD1672 is low-cost, low-power upgrade for AD1671**

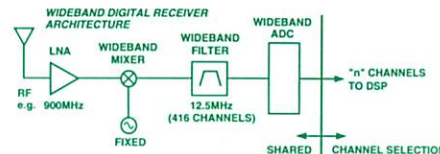
The AD1672 is a 12-bit, single-supply, 3-MSPS ADC with low power consumption, wideband input sample-and-hold, on-chip reference, and an attractive performance/price ratio. It uses a multistage pipelined architecture with output error correction for 12-bit accuracy at 3-MSPS data rates, with a guarantee of no missing codes over the industrial temperature range (-40 to +85°C).

At 240 mW (363 max), the AD1672 uses a fraction of the power of many other available solutions. It has pin-strappable input ranges of 2.5 and 5 V unipolar (binary), and  $\pm 2.5$  V bipolar (offset binary). Output data is available in a parallel format. An out-of-range bit is available to indicate excessively high input.

Applications include PHS basestations, IR imaging systems, sonar, and desktop scanners. Salient specifications include 68-dB SINAD and 77-dB SFDR (63 and 65 min at 500 kHz). Analog bandwidth is 5 MHz full-power and 20 MHz small-signal. The device can use its on-chip 2.5-V reference or an external reference—and can provide a system reference. The AD1672 is housed in a 28-pin PLCC. ▶

### 12-Bit, 41-MSPS A/D

**Has 80-dB SFDR to 20 MHz, 68-dB SNR, 100-MHz BW**



The AD9042 is a high-speed, low-power, high-performance monolithic 12-bit analog-to-digital converter (ADC). All necessary functions, including track-and-hold and reference, are included on the chip to provide a complete conversion solution. The AD9042 runs off a single +5-volt supply and provides CMOS-compatible parallel digital outputs at 41 MSPS.

Designed specifically to address the needs of wideband, multi-channel receivers [see *Analog Dialogue* 29-2, pp. 11-12], the AD9042 maintains 80-dB spurious-free dynamic range (SFDR) over a bandwidth of 20 MHz. Noise performance is also exceptional, with typical signal-to-noise ratio of 68 dB.

Typical applications requiring the AD9042's kind of performance are found in cellular/PCS base stations, GPS anti-jamming receivers, communications receivers, spectrum analyzers, medical imaging, and automatic test equipment.

Other aspects of the AD9042's performance include analog input bandwidth of 100 MHz, differential nonlinearity of  $\pm 0.3$  LSB, and integral nonlinearity of  $\pm 0.75$  LSB. The specified SFDR can be further improved (>90 dB) through the use of dither to essentially randomize the input signal with respect to the major transitions of the transfer function, where the largest errors appear. See application note AN-410.\*

The AD9042 requires a maximum of 147 mA at +5 V, or 735 milliwatts, and typically about 600 milliwatts. It is packaged in a 28-pin ceramic DIP, and a 44-pin TQFP will be available. The data sheet includes instructions for constructing and using evaluation boards; they may also be purchased. ▶

\*For AN-410, Request 15

**A/D Converter Comparison**

	AD9042AD/AST	AD1672AP	AD9050BR/BRS
Supply voltage (V)	5	5	5
Resolution (bits)	12	12	10
Sampling rate (MSPS)	41	3	40
Output format	Parallel (2s complement)	Parallel	Parallel (offset bin)
Signal to noise-and-distortion (SINAD), dB min			
500 kHz		63 (68 typ)	
1.2 MHz	64 [25°C] (67.5 typ)		
1.5 MHz		67 (typ)	
2.3 MHz			55.5 typ (25°C)
10.3 MHz			53 [25°C] (55 typ)
19.5 MHz	64 [25°C] (67 typ)		
Spurious-free dynamic range (SFDR), dBFS	81 @ 19.5 MHz	77 at 500 kHz	NS
Missing codes (over temperature, guaranteed)	None	None	None
On-chip voltage reference	2.4 V	2.5 V	2.5 V
Analog input bandwidth (MHz)	100	5, 20-SS†	100
Operating temperature range	-40 to +85°C	-40 to +85°C	-40 to +85°C
Supply current, max, mA	147	69	80
Power requirement, max, mW	735 (595 typ)	363 (240 typ)	400 (315 typ)
Package(s)	ceramic DIP, TQFP-44	PLCC-28	SO, SSOP-28
Evaluation board	AD9042D/PCB, ... ST/PCB	AD1672-EB	AD9050/PCB
Evaluation board price	\$350, \$150	\$150	\$250
Device price (1000s)	\$199, \$83.30	\$29.90	\$19.90
Faxcode*	1922	1880	1843

\*For data sheets, use ADI's web site: <http://www.analog.com> or AnalogFax™ 24-hour automated delivery system: (800) 446-6212

†SS: Small signal

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## Temperature-to-Digital IC; Signal-Conditioning Modules

### F/V Converters

**5B45 & 5B46 modules have 1500-V rms isolation**



The 5B45 and 5B46 are frequency-to-voltage converters for use in 5B-series modular signal-conditioning systems. They accept inputs in the form of logic signals, or a wide variety of zero-crossing waveforms, and provide output voltage (0 to +5 V) proportional to the input frequency. Applications include tachometers, flowmeters, optical encoders, motor control and speed monitoring, line-frequency monitoring, and fluid-flow measurements and control.

5B systems of compact, low-cost signal-conditioning modules have been in use in industry for a decade (*Analog Dialogue* 20-2, 1986, pp. 8-9) and are widely emulated. Like many of the other 5B modules, the 5B45/46 are input/output isolated (1500-V rms), and have 240-V rms input protection. The five standard members of the 5B45 family measure frequencies with full-scale ranges from 500 Hz to 10 kHz, and the four 5B46s handle ranges from 25 kHz to 250 kHz. Custom ranges are also available.

Performance characteristics include accuracy to within 0.1% of span, nonlinearity  $< \pm 0.015\%$  of span, Offset drift of  $\pm 20 \mu\text{V}/^\circ\text{C}$  and gain drift of  $\pm 20 \text{ ppm}/^\circ\text{C}$  over the operating range of  $-40$  to  $+85^\circ\text{C}$ . Common-mode rejection is 120 dB, and response to step frequency changes is fast, e.g., a full-span 1-kHz step (5B45-02) is measured to within 0.1% in 140 ms.

They plug into industry-standard 5B mix-and-match backplanes and require +5-volt power. Prices in 100s: \$126.

Faxcode 7030

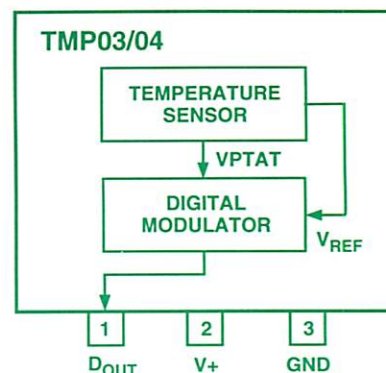
### IC Serial-Digital-Output Thermometers

**TMP03/04 function as remote 3-wire temp sensors**  
**Single +5-V supply, open collector or logic output**

The TMP03 and TMP04 3-pin temperature detectors generate a modulated serial digital output whose clock-independent mark-space ratio varies in direct proportion to the output of the device's temperature sensor. They differ only in output circuit: the TMP03 has an open-collector output, and the TMP04 has a CMOS/TTL-compatible voltage output.

The ratiometric encoding format of the serial digital output is independent of the clock-drift errors common to most serial modulation techniques, such as voltage-to-frequency converters. Overall accuracy is to within  $\pm 1.5^\circ\text{C}$  (typical) from  $-25^\circ\text{C}$  to  $+100^\circ\text{C}$ , with  $0.5^\circ$  nonlinearity. Operation is specified at supply voltages from 4.5 V to 7 V. At +5 V, supply current (unloaded) is less than 1.3 mA.

The TMP03's open collector, which can sink up to +5 mA, is best suited for circuits utilizing



optocouplers or isolation transformers. The TMP04 is easily interfaced to the serial inputs of most popular microprocessors. The devices are available in SO-8 and will soon be available in TO-92 and TSSOP-8 packages. Prices start at \$2.49 in 1000s.

Faxcode 1850\*

## Conditioners for Thermocouples, RTDs

**7B27 module conditions J,K,T,E,R,S,B; 5 or 10 V out**  
**7B14 linearizes 100- $\Omega$  Pt, 120- $\Omega$  Ni, 10- $\Omega$  Cu RTDs**

The 7B27 and 7B14 are new modules for use in Analog Devices 7B-Series modular signal-conditioning systems (see *Analog Dialogue* 27-1, 1993, pp. 9-11). The 7B Series signal conditioners are compact, low-cost, high-performance analog-input and -output signal-conditioning modules (usually with high-voltage input-output isolation). They are designed to plug into sockets on a suitable backplane available from Analog Devices or provided by the user. 7B Series analog input modules provide conditioning for RTDs, thermocouples, millivolt and voltage sources, and process-current signals. Output modules translate high-level signals to process currents or voltages.

The new 7B27 and 7B14 provide very low-cost signal conditioning for thermocouples and RTDs. Applications include process monitoring & control, and test & measurement, as well as energy management

and SCADA (supervisory control and data acquisition), in locations where high-voltage isolation is not a requirement. (The 7B37 and 7B24 are available for high-isolation applications.)

The various options of 7B27 accept inputs from all standard thermocouples, provide cold-junction compensation, and provide outputs at the 0 to 5 or 0 to 10-V level. Accuracy is to within  $\pm 0.1\%$  of span, nonlinearity is  $\pm 0.02\%$  of span, response time is 150 ms to 90% of a step change. Common-mode voltage rating is 100 V rms continuous with 160 dB of CMR at 50/60 Hz. Inputs are protected for up to  $\pm 30$  V dc continuous. The 7B14 family provide conditioning (except for isolation) for platinum, nickel, and copper RTDs with accuracies from  $\pm 0.03\%$  to  $\pm 1\%$  of span.

The 7B27 and 7B14 are priced (1s) at \$85. Faxcodes\*: 7038 and 7035

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\*For immediate data, use ADI's web site: <http://www.analog.com> or ADI's 24-hour AnalogFax™ line, 1 (800) 446-6212; use Faxcode.



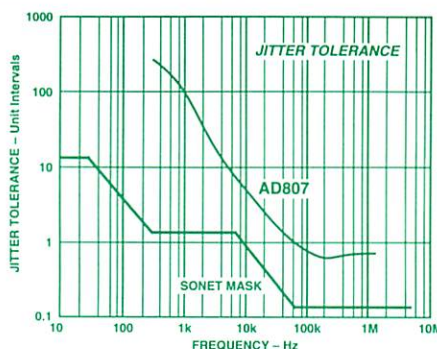
## A Mixed Bag

### F-O Receiver, Frequency Synthesizer

**AD807 has quantizer, clock recovery, data retiming**  
**AD809 synthesizes 155.52 MHz from 19.44 or 9.72 MHz**

The AD807 fiber optic receiver provides in a tiny package the key functions of data quantization, signal level-detection, clock recovery and data retiming for 155-Mbps non-return-to-zero (NRZ) data. With a PIN diode and preamplifier (for example, using the AD8015 transimpedance amplifier), it can provide a highly integrated, high-performance, low-cost, low power fiber-optic receiver for SONET OC-3 or SDH STM-1 line interface circuits. It has only 2.0° of jitter (2.7° max for a 2<sup>23</sup>-1 PRN sequence) and high jitter tolerance (see illustration).

The AD809 provides a 155.52-MHz ECL/PECL output clock from either a 19.44-MHz or a 9.72-MHz TTL/CMOS/ECL/PECL reference frequency. Output jitter is only 1.6° rms (2.9 max). The low-jitter VCO, low power (90 mW), and wide operating temperature range make it suitable for generating a 155.52-MHz bit clock for



transmission in SONET/SDH Fiber in the Loop systems.

The AD807 and AD809 are specified for the -40 to +85°C temperature range and are housed in 16-pin narrow-body SOICs. Single-supply devices, they operate at +5 or -5.2 V. Prices for the AD807/AD809 start at \$17.80/\$13.25 in 1000s.

**Faxcodes 1904 and 1935\***

### Voltage References

**REF191/198: 2.048/4.096 V**  
**0.5 or 1 mV/LSB (12 bits)**

The REF191 and REF198 are low-cost, low-power precision voltage references designed for easy scaling of A/D and D/A converters. The REF191 has a nominal output voltage of 2.048 V (0.5 mV per LSB in 12-bit converters); and the REF198 has a nominal output of 4.096 V (1 mV/LSB). The REF191 is intended for 3-V systems operating down to a minimum of 2.7 V; and the REF198 is for 5-V systems operating down to 4.5 V.

E, F, and G versions offer maximum error specs of ±2, ±5, and ±10 mV, with max tempcos of 5, 10, and 25 ppm/°C. Quiescent current is 45 µA max (15 µA max in Sleep mode). Short-circuit-protected, they can supply output current up to 30 mA and are specified for -40 to +85°C. Packages include 8-pin SOIC, TSSOP, and plastic DIPs. Pricing (1000s) begins at \$1.91.

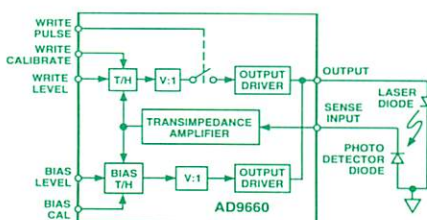
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### 200-MHz Laser-Diode Driver IC

**AD9660 has on-board light-power control loops**  
**Useful for optical disk drives, printers & Copiers**

The AD9660 is a highly integrated driver for laser-diode applications, such as optical disk drives, printers, and copiers. Using a 5-volt supply, it provides two calibrated sourcing output currents: up to 90 mA for bias and 60 mA for modulation ("Write"). An uncalibrated offset current is also available. Output power is calibrated by two analog feedback loops via two analog inputs. Calibration and output control are TTL/CMOS-compatible.

Output rise and fall times are typically 1.5 and 2.0 ns, respectively—a response time fast enough to allow for pulsewidth modulation for gray scale image enhancement. When the device is not in use, a Disable circuit turns off the output drivers.



The AD9660 can also be used in continuous closed-loop operation, in which the output power level follows an analog Write Level voltage input. With optimized choice of photo detector and external hold capacitor, the Write loop can achieve bandwidths as high as 25 MHz.

The AD9660, packaged in a 28-pin plastic SOIC, operates from 0 to +70°C. Price (100s) is \$9.75. **Faxcode 1906\***

### V-Doubler/Inverters

**Charge-pump based**  
**ADM660/8660: 100-mA I<sub>out</sub>**

The ADM660 and ADM8660 are charge-pump voltage converters; with a pair of 10-µF external capacitors, they can generate an inverted supply voltage,  $V_{OUT} = -V_{IN}$ , with respect to common. The difference between  $V_{OUT}$  and  $V_{IN}$  is of course double  $V_{IN}$ , but the ADM660 can be connected to furnish a doubled supply voltage, *relative to common*.

Inputs from +1.5 to +7 V can be inverted to -1.5 to -7 V; output currents of up to 100 mA at -5 V are available. If a charge pump frequency of 120 kHz is chosen, the capacitors can be reduced to 2.2 µF. The ADM8660 includes a shutdown function to disable the device and reduce the quiescent current from 600 µA to 300 nA. Both devices operate from -40 to +85°C and are packaged in 8-pin DIPs and SO. Prices (100s) for ADM660/8660 are \$1.90/\$2.00. **Faxcode 1934\***

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\*For immediate data, use ADI's web site: <http://www.analog.com> or ADI's 24-hour AnalogFax™ line, 1 (800) 446-6212; use Faxcode.



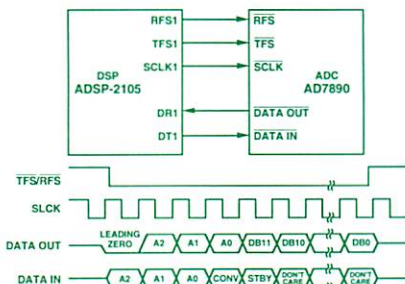
# Ask The Applications Engineer—19

## INTERFACING TO SERIAL CONVERTERS—I

by Eamon Nash

*Q. I need data converters to fit in a tight space, and I suspect that a serial interface will help. What do I need to know to choose and use one?*

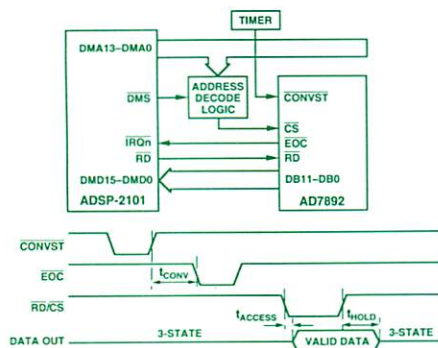
**A.** Let's start by looking at how a serial interface works and then compare it to a parallel interface. In doing this we will dispel some myths about serial data converters.



The figure shows an AD7890 8-Channel multiplexed 12-bit serial A/D converter (ADC) connected to the serial port of an ADSP-2105 digital signal processor (DSP). Also shown is the timing sequence that the DSP uses to communicate with the ADC. The 12 bits that constitute the conversion result are transmitted as a serial data stream over a single line. The data stream also includes three additional bits that identify the input channel that the AD7890's multiplexer is currently selecting. To distinguish the bits of the serial data stream from one another, a clock signal (SCLK) must be provided, usually by the DSP; However, sometimes the ADC supplies this clock as an output. The DSP usually (but not always) supplies an additional framing pulse that is active either for one cycle at the beginning of the communication or, as shown (TFS/RFS), for the duration of the transmission.

In this example, the DSP's serial port is used to program an internal 5-bit register in the ADC. The register's bits control such functions as selecting the channel to be converted, putting the device in power-down mode, and starting a conversion. It should be evident that the serial interface, in this case, must be bi-directional.

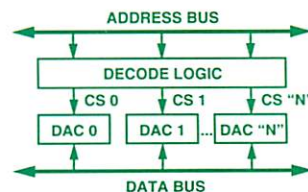
A parallel ADC, on the other hand, connects directly (or possibly through buffers) to the data bus of the processor it is interfaced with. The figure shows the AD7892 interfaced to an ADSP-2101. When a conversion is complete, the AD7892 interrupts the DSP, which responds by doing a single read of the ADC's decoded memory address.



The key difference between serial and parallel data converters lies in the number of interface lines required. From a space saving point of view, serial converters offer a clear advantage because of reduced device pin-count. This makes it possible to package a 12-bit serial ADC or DAC in an 8-pin DIP or SO package. More significantly, board space is saved because serial interface connections require fewer PCB tracks.

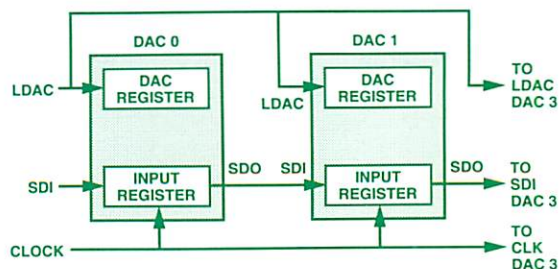
*Q. My digital-to-analog converters have to be physically remote from the central processor and from one another. What is the best way to approach this?*

**A.** Initially, you must decide whether to use serial or parallel DACs. With parallel DACs, you could map each one into a memory mapped I/O location, as shown in the figure. You would then program each DAC by simply doing a Write command to the appropriate I/O location. However, this configuration has a significant disadvantage. It requires a parallel data bus, along with some control signals, to all of the remote locations. Clearly, a serial interface, that can have as few as two wires, is much more economical.



Serial converters cannot in general be mapped into a processor's memory. But a number of serial DACs could be connected to the serial I/O port of the processor. Then, other ports on the processor could be used to generate Chip Select signals to enable the DACs individually. The Chip Select signals will require a line from each device to the interface. But there may be a limit to the number of lines on the processor that can be configured to transmit Chip Select signals.

One way of getting around this problem is to use serial DACs that can be daisy-chained together. The figure shows how to connect multiple DACs to a single I/O port. Each DAC has a Serial Data Out (SDO) pin that connects to the Serial Data In (SDI) pin of the next DAC in the chain. LDAC and SCLK are fed in parallel to all the DACs in the chain. Because the data clocked into SDI eventually appears at SDO (N clock cycles later), a single I/O port can address multiple DACs. However, the port must output a long data stream (N bits per DAC times the number of devices in the chain). The great advantage of this configuration is that device decoding is not needed. All devices are effectively at the same I/O location. The main drawback of daisy chaining is accessibility (or latency). To change the state of even a single DAC, the processor must still output a complete data stream from the I/O port.



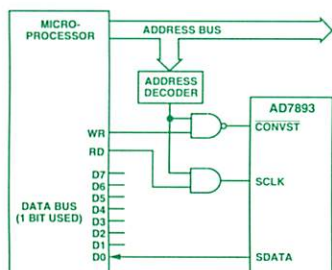


*Q. If serial data converters save so much space and wire, why aren't they used in every space-sensitive application?*

**A.** A major disadvantage of serial interfacing is the tradeoff of speed for space. For example, to program a parallel DAC, just place the data on the data bus and clock it into the DAC with a single pulse. However, when writing to a serial DAC, the bits must be clocked in sequentially ( $N$  clock pulses for an  $N$ -bit converter) and followed by a Load pulse. The processor's I/O port spends a relatively large amount of time communicating with a serial converter. Consequently, serial converters with throughput rates above 500 ksp/s are uncommon.

*Q. My 8-bit processor doesn't have a serial port. Is there a way to interface a serial 12-bit ADC like the AD7893 to the processor's parallel bus?*

**A.** It can of course be done using an external shift register, which is loaded serially (and asynchronously), then clocked into the processor's parallel port. However, if the sense of the question is "without external logic", the serial ADC can be interfaced as if it were a 1-bit parallel ADC. Connect the converter's SDATA pin to one of the processor's data bus lines (it is connected to D0 in the diagram). Using some decode logic, the converter can be mapped into one of the processor's memory locations so that the result of the conversion can be read with 12 successive Read commands. Then additional software commands integrate the LSBs of the 12 bytes that were read into a single 12-bit parallel word.



This technique, which is sometimes referred to as "bit banging", is very inefficient from a software perspective. But it may be acceptable in applications in which the processor runs much faster than the converter.

*Q. In the last example, a gated version of the processor's write signal was used to start conversions on the AD7893. Are there problems with that approach?*

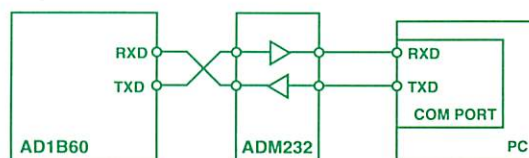
**A.** I am glad you spotted that. In this example, a conversion can be initiated by doing a dummy write to the AD7893's mapped memory location. No data is exchanged, but the processor provides the write pulse needed to begin the conversion. From a hardware perspective, this configuration is very simple because it avoids the need to generate a conversion signal.

However, the technique is not recommended in data-acquisition applications, in which signals must be sampled periodically. Even if the processor is programmed to do periodic writes to the ADC, phase jitter on the Write pulse will seriously degrade the attainable signal-to-noise ratio (SNR). The gating process may make the Write signal jitter even worse. A sampling clock phase jitter level of as little as 1 ns, for example, would degrade the SNR of an ideal 100-kHz sine wave to about

60dB (less than 10 effective bits of resolution). There is also an additional danger that overshoot and noise on the sampling signal will further degrade the integrity of the analog to digital conversion.

*Q. When should I choose a converter with an asynchronous serial interface?*

**A.** An asynchronous link allows devices to exchange unclocked data with each other. The devices must initially be programmed to use the identical data formats. This involves setting a particular data rate (usually expressed in baud, or bits per second). A convention, that defines how to initiate and end transmissions, is also necessary. We do this using identifiable data sequences called *start* and *stop* bits. The transmission may also include *parity* bits that facilitate error detection.



The figure shows how the AD1B60 Digitizing Signal Conditioner interfaces to a PC's asynchronous COM Port. This is a 3-wire bidirectional interface (the ground lines have been omitted for clarity). Notice that the receive and transmit lines exchange roles at the other end of the line.

An asynchronous data link is useful in applications in which devices communicate only sporadically. Since start and stop bits are included in every transmission, a device can initiate communication at any time by simply outputting its data. The number of connections between devices is reduced because clocking and control signals are no longer necessary.

*Q. The data sheet of an ADC I am considering recommends using a non-continuous clock on the serial interface. Why?*

**A.** The specification probably requires that the clock be kept inactive while the conversion is in progress. Some ADCs require this because a continuous data clock can feed through to the analog section of the device and adversely affect the integrity of the conversion. A continuous clock signal can be discontinued during conversion if the I/O port has a framing pulse; it is used as a gating signal that enables the serial clock to the converter only during data transfer.

*Q. What makes a device SPI or MICROWIRE compatible?*

**A.** SPI (Serial Peripheral Interface) and MICROWIRE are serial interface standards developed by Motorola and National Semiconductor, respectively. Most synchronous serial converters can be easily interfaced to these ports; but in some cases additional "glue" logic may be necessary.

*Q. O.K. I decided to put prejudice aside and use a serial ADC in my current design. I have just wired it up as the data sheet specifies. When my micro reads the conversion result, the ADC always seems to output FFF<sub>HEX</sub>. What's happening?*

**A.** Perhaps you are having a communications problem. We need to look at the connections between the ADC and the processor—and at how the timing and control signals have been set up. We also need to look at the Interrupt structure. The next installment will return to this issue, discussing the problems encountered when designing serial interfaces. ►



## Worth Reading

### CATALOG

**Signal Conditioning and Data Acquisition Solutions Catalog** 248 colorful pages of module and board-level subsystem solutions for process monitoring and control, test and measurement, machinery monitoring, and data acquisition from Analog Devices Iomation. Includes 2B, 3B, 5B, 6B, and 7B Series of signal-conditioning modules, and RTI Series of computer interfacing boards. **Free. Request 2**

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**DSPatch—The DSP Applications Newsletter: Number 34**, Fall, 1995. Features AD1843 codec; Analog Devices participation in ICSPAT/DSP World Conference on Signal Processing; LITEF GmbH's Secure Voice Module; Real Time Signal Processing's Integrated Development Environment (IDE) for ADI's EZ-KIT Lite; Signion Systems DSP-based Solid State All-Electronic Energy Meter (SALEM); plus Q&A on applying ADSP-2181. Brief notes on Tartan compilers for SHARC, Spectron porting SPOX OS to SHARC, Real Time Systems, Inc. Talisman PC add-in boards, connecting ADSP-2105 to a host through shared memory, & much more. 16 pp. **Request 3**

**ANALOG BRIEFINGS—The newsletter for the defense/aerospace industry: Volume 10, No. 2, October, 1995.** Features articles on: A new high-density dc-to-dc converter with integral EMI filtering; Products and processes for a changing aerospace marketplace; Multichip modules increase functionality in small places; and Tartan, Inc. partnership with ADI on SHARC compilers; plus new products and new Standard Microcircuit Drawings. 8 pp. **Request 4**

**COMMUNICATIONS DIRECT—Systems and IC solutions for demanding markets: Newsletter: Vol. 1, No. 2, October, 1995.** Features include: ADSL chipset sends 8 MBPS down phone lines; Technical brief—Getting information down the line; RF designers are from Mars—IC designers are from Venus; and more. 8 pages. **Request 5**

### BROCHURES AND GUIDES

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**Applications of the SSM2120 Dynamic Range Processor**, by Joe Buxton. Includes details of evaluation board. [12 pp., AN-382]. **Request 10**

**Electrically induced damage to standard linear integrated circuits: The most common causes and the associated fixes to prevent recurrence**, by Niall Lyne. Introduction; Electrostatic discharge, ESD models, prevention; Latch up, design rules, prevention; High-voltage transients, typical applications of

transient voltage suppressors; Summary; References [8 pp., AN-397]. **Request 11**

**Considerations for selecting a DSP—Why buy the ADSP-21060? (SHARC vs. TMS320C40).** Includes descriptions, architecture block diagrams, comparisons, 14 tables. [20 pp., AN-403]. **Request 12**

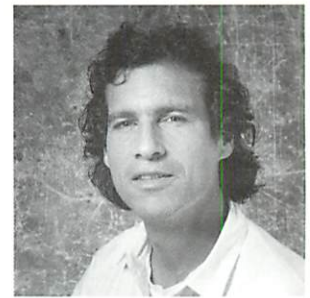
**Considerations for mixed-signal circuit board design (How to design a PCB layout/assembly compatible with the AD1845 and CS4231 codecs).** Introduction; Using a codec on your PCB; Cost vs. performance design; Conclusion; References. [8 pp., AN-404]. **Request 13** 

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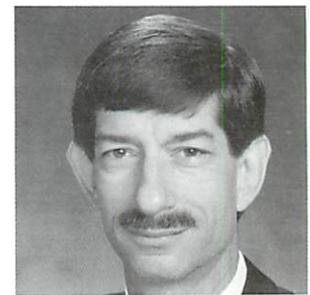
**Dave Quinn** (page 11), a Product/Test Group Leader in ADI's Advanced Linear Product group, has worked on trim and test solutions for instrumentation amps, accelerometers, temperature transducers, Hall cells, and high-speed op amps. He led a team in the development of hardware and software to use optical character recognition techniques for testing and traceability. His hobbies include automobiles, photography, and—lately—building his home.




**Steve Sherman** (page 11), a Senior Design Engineer in the accelerometer group at Analog Devices for the past 6 years, had designed circuits for the linear group during the previous 11 years. Earlier, he designed custom digital ICs for mainframes at Burroughs and developed IC fabrication processes for high-speed bipolar circuits at DEC. He was born in Woonsocket, RI, earned a BSEE at URI and an MSEE at Case Western Reserve. He likes to take long walks on the beach (but doesn't like to go into the water).



**Steve Sockolov** (page 13) is the Strategic Marketing Manager for amplifiers and comparators in ADI's precision amplifier product line. He has a BSEE from California State University (San Diego), has worked at several semiconductor companies, and has written numerous articles for a variety of publications. His hobbies include mountain biking and studying foreign languages.



**Eamon Nash** (page 20) is a Senior Applications Engineer, now at ADI's Advanced Linear Products group and formerly at the Central Applications group. He was graduated from the University of Limerick, Ireland, with a Bachelor of Engineering degree in Electronics. His spare-time activities include tennis, squash, and rollerblading. 



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A/D Converter, 12-bit, 41 MSPS, 575 mW @ +5 V, 80-dB SFDR at Nyquist, 90-dBFS IMD	AD9042	1922
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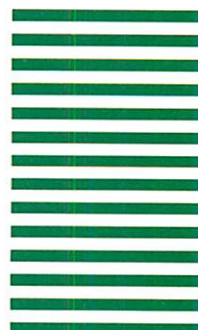
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